HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12531C

BUFFERED TELEPRINTER INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assembly:
12531-60022, Rev. 1117, 1120, and 1204

12531-90033

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

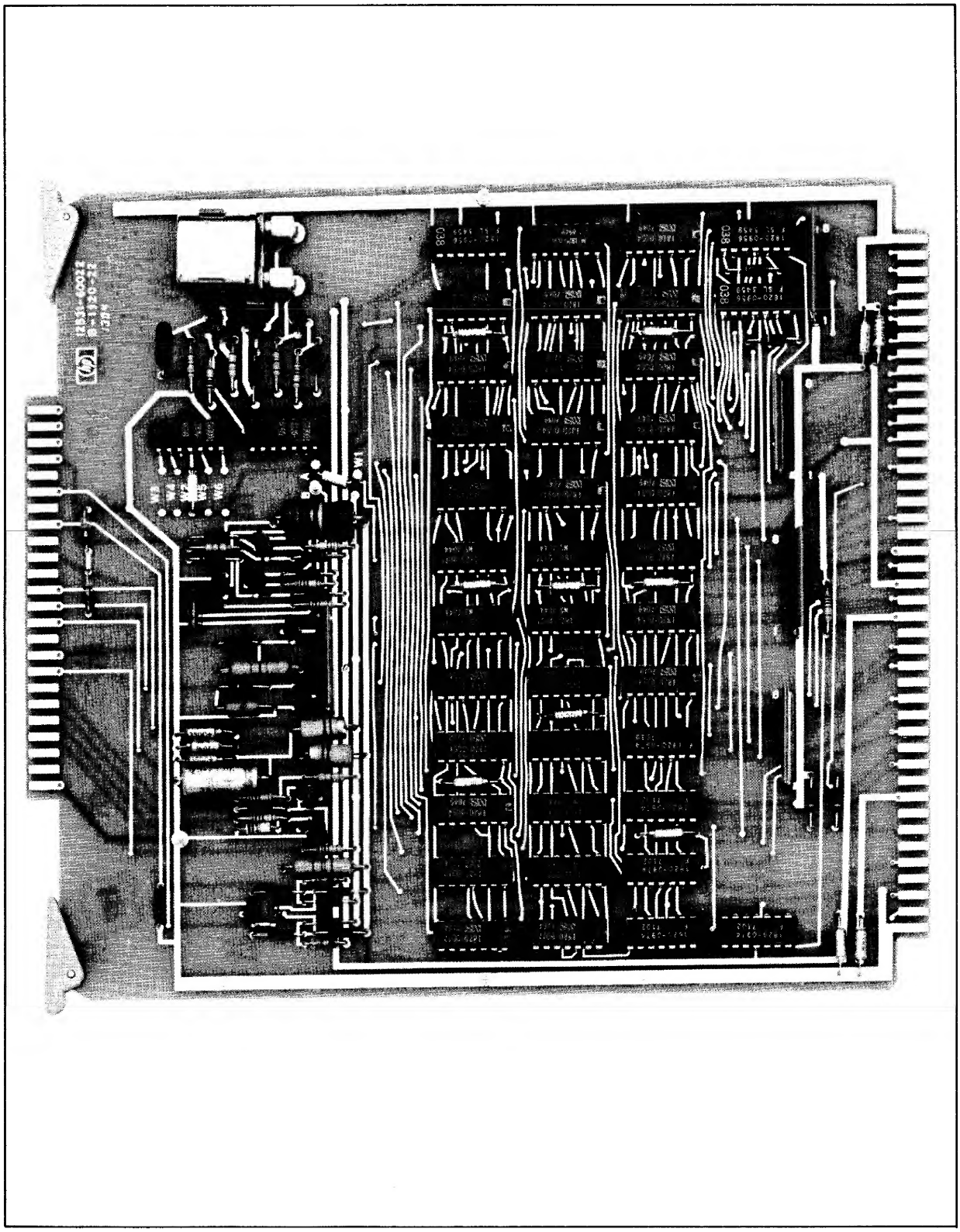


Figure 1-1. 12531C Buffered Teleprinter Interface Card

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, troubleshooting information, and replaceable parts information for the Hewlett-Packard (HP) 12531C Buffered Teleprinter Interface Kit.

1-3. DESCRIPTION.

1-4. GENERAL.

1-5. The circuit card in the interface kit controls data transfer between an HP computer and an HP 2752A or 2754B Teleprinter. In this manual, the term "teleprinter" signifies either of these two teleprinter models. The terms "circuit card", "interface card", or "card" indicate the circuit card supplied in the kit.

1-6. As well as being used with the above teleprinters, interface kit options 001 and 002 allow the interface kit to be used with Electronic Industries Association (EIA) compatible devices. Option 001 is used with devices such as the HP 2749A Teleprinter or HP 2600A Keyboard-Display Terminal. Option 002 is used with data modems such as the Bell model 103A Data-Phone. A jumper wire on the card allows the selection of five different rates of data transfer to permit use of the card with various I/O devices. A second jumper wire on the card can be connected to allow an external clock pulse, supplied by the I/O device, to control the rate of data transfer.

1-7. The interface card installs in the computer cabinet or in the cabinet of an I/O extender, and can be used with the HP 2100, 2114, 2115, or 2116 Computer.

1-8. KIT CONTENTS.

1-9. The 12531C Buffered Teleprinter Interface kit contains one each of the following:

a. Buffered teleprinter interface card (part no. 12531-60022), illustrated in figure 1-1.

b. Operating and service manual (part no. 12531-90033).

1-10. IDENTIFICATION FEATURES OF KIT AND CONTENTS.

1-11. KIT. Five digits and a letter (00000A) are used to identify standard interface kits used with HP computers. The five digits identify the kit; the letter indicates the revision level of the kit.

1-12. CIRCUIT CARD. The circuit card supplied with the kit is identified by a part number marked on the card. In addition to a part number, the card is further identified by a letter, a revision code, and a division code (e.g., B-1117-22). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The revision code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. The division code (one or two digits) identifies the HP division which manufactured the card.

1-13. If the revision code stamped on the buffered teleprinter interface card does not agree with the revision codes on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-14. OPERATING AND SERVICE MANUAL. The manual supplied with the kit is identified by its name and part number. The part number, 12531-90033, is printed in the lower left corner of the manual cover. The publication date is printed in the lower right corner. If the manual is revised, the publication date on the cover is changed.

1-15. SPECIFICATIONS.

1-16. Table 1-1 lists the specifications of the 12531C Buffered Teleprinter Interface Kit. In the table and throughout this manual the term "character" signifies an 8-bit, 10-bit, or 11-bit word handled by the interface card. In the case of data sent to the printer portion of the teleprinter, each character results in the typing of a letter of the alphabet, a digit, or a symbol, or the character causes actuation of such typewriter mechanical functions as carriage return or a bell stroke. When a character is sent to the punch portion of the teleprinter, the eight data bits involved are punched in the tape. When receiving data from the teleprinter keyboard, a character is supplied each time a key is pressed. When a character is furnished by the teleprinter tape reader, a character is received for each set of holes read in the tape.

Table 1-1. Specifications

ITEM	SPECIFICATIONS
Character code, computer output*:	
Teleprinter tape punch	Any 8-bit character.
Teleprinter print unit	Eight-bit ASCII code (including parity bit), modified for HP use.
I/O devices other than teleprinter	Any 8-bit character the I/O device is capable of accepting.
Character code, computer input**:	
Teleprinter tape reader	Any 8-bit character.
Teleprinter keyboard	Eight-bit ASCII code, modified for HP use, with even parity. Early models of the 2752A Teleprinter did not have the parity feature; the parity bit is logic 0 if not used.
I/O devices other than teleprinter	Any 8-bit character the I/O device is capable of furnishing.
Parity Check:	When the I/O device is the teleprinter, no parity check is made by the hardware. If desired, a parity check of inputs from the teleprinter keyboard or teleprinter tape reader can be made by the software.
Data transfer rate:	
Using internal clock pulse	Data transfer rate is 110, 220, 440, 880, or 1760 bits per second, depending on whether jumper W2, W3, W4, W5, or W6 is installed on the interface card. For the teleprinter, W2 is used and the transfer rate, in terms of characters, is 10 characters per second for the teleprinter tape reader unit. For keyboard operations, character transfer rate is determined by the speed of typing. For the teleprinter print and punch units, character transfer rate is determined by the computer program, and must not exceed 10 characters per second.
Using external clock pulse	For computer input, maximum character transfer rate is 1/80th of the clock pulse frequency. For computer output, maximum rate is 1/88th of the clock pulse frequency. These rates decrease if characters are supplied at a slower rate by the I/O device or computer.
Voltage levels:	
Signal level, interface card to Bell Model 103A Data-Phone	Logic 1, -3 to -20V dc Logic 0, +3 to +20V dc
Signal level, Bell Model 103A Data-Phone to interface card	Logic 1, -11 to -13V dc Logic 0, +11 to +13V dc
Current required from computer by interface card†	
+4.5V dc	0.76A
-2V dc	0.05A
+12V dc	0.05A
-12V dc	0.10A

* In a computer output operation, 8-bit characters are transferred in parallel from the computer to the interface card. There, one start bit and one or two stop bits are added, and the resulting 10 or 11 bits are transferred in serial to the teleprinter.

** In a computer input operation, 11-bit or 10-bit characters are transferred serially from the I/O device to the interface card. There, a start bit, and one or two stop bits are discarded. The resulting 8-bit word is transferred in parallel to the computer A- or B-register.

† Includes +12 volt and -12 volt current from the interface card to the teleprinter.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspecting, installing, and checking the operation of the interface kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the interface kit is ordered with a computer, the kit is installed at the factory. When this is the case, it is necessary only to check operation of the teleprinter, together with the interface card, after the computer and teleprinter are installed. Checkout instructions are furnished in paragraph 2-17.

2-5. If the interface kit is ordered separately, inspect the carton containing the kit before opening it. If there is evidence of damage, if water stains are visible, or if the box rattles, request that the carrier's agent be present when the box is opened.

2-6. Inspect each portion of the kit as the parts are unpacked. Look for such damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the kit is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier. (HP Sales and Service Offices are listed at the back of this manual.)

2-7. After inspecting all components, refer to paragraph 1-9 of this manual and ensure that the kit is complete. Also check the part numbers given in paragraph 1-9 against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

2-8. PREPARATION FOR INSTALLATION.

2-9. COMPUTATION OF CURRENT REQUIREMENTS.

2-10. The circuit card in the interface kit obtains its operating voltages from the computer power supply. Before installing the card, it is necessary to determine whether the added current will overload the power supply. (If the circuit card was installed at the factory, the required calculations have been made, and it has been determined that overload will not occur.) The current requirements of the interface card are listed in table 1-1. Included is the +12- and -12-volt current forwarded from the interface card to the teleprinter.

2-11. If current requirements exceed the capabilities of the computer power supply, an HP power supply extender or I/O extender must be installed.

2-12. JUMPER WIRE CONNECTIONS.

2-13. The interface card has three jumper wires, which are shown in figure 5-2. If the card is supplied as part of a computer system, the jumper wires are connected to suit the I/O device with which the card is used. If the card is not supplied as part of a computer system, the jumpers are connected for use with a teleprinter. For the teleprinter, one jumper is used in position W1, and is connected to terminal A, to permit the clock pulse generated on the interface card to be employed. Another jumper is connected in position W2 to select a data transfer rate of 110 bits per second, which is required for the teleprinter.

2-14. If the circuit card is used with an I/O device other than the teleprinter, and the card is not received in a computer, the jumpers must be connected to suit the device. If the I/O device furnishes a clock pulse to the interface card, the jumper used in position W1 is connected to terminal B, rather than terminal A. If the clock on the interface card is to be used, jumper W1 must be connected to terminal A and the other jumper (W2) is connected in position W2, W3, W4, W5, or W6, to select respectively 110, 220, 440, 880, or 1760 bits per second, to suit the data transfer rate of the I/O device. Jumper W7 provides the number of stop bits required by the I/O device. Position A provides two stop bits (11-bit character); position B provides one stop bit (10-bit character).

2-15. INSTALLATION.

2-16. After ensuring that the computer power supply can handle the added load, and after the two jumper wires are correctly connected, install the circuit card in the following manner:

a. Install the computer and teleprinter or other I/O device, if these have not been installed.

b. Determine the I/O select code to be used for the teleprinter or other I/O device, and the I/O interface card slot to which the select code corresponds.

c. Turn off power at the computer and I/O device. Install the circuit card in the required card slot in the computer I/O extender. Components on the card must be on the same side of the card as for other cards in the I/O interface slots. When inserting, exercise care not to damage components or traces on the card or on adjacent cards. Press the circuit card firmly into place.

d. The I/O device has a cable with a connector which fits on the end of the interface card. Pass the cable into the computer or I/O extender and plug the connector on the end of the interface card.

2-17. CHECKOUT.

2-18. To verify operation of the interface card, perform the on-line diagnostic test for the I/O device connected to the card. Operating procedures for diagnostic tests are described in the *Manual of Diagnostics*. If the interface card is used with a teleprinter and a 2116-series computer, use procedure part number 5951-1368. For a teleprinter and a 2114- or 2115-series computer, use procedure part number 5951-1367. For a teleprinter and a 2100-series computer, use procedure part number 5951-1365.

2-19. RESHIPMENT.

2-20. If an item of the kit is to be shipped to Hewlett-Packard for repair, attach a tag to the item identifying the owner and indicating the service to be performed. Include the interface kit number.

2-21. Pack the item in the original factory packing material. If the original material is not available, standard factory packing material can be obtained from the nearest HP Sales and Service Office.

2-22. If standard packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorn, N.J.) or equivalent and place in a corrugated carton (200-pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

SECTION III

PROGRAMMING

3-1. INTRODUCTION.

3-2. This section describes assembly-language programming procedures for the 12531C interface card and its associated I/O device. It should be noted that in many instances I/O routines in the HP program library can be used in place of specially written routines. Information on the library routines is provided in the Hewlett-Packard Program Catalog (part no. 5950-9226).

3-3. The programming discussion which follows deals with the teleprinter. The explanation also applies to other I/O devices used with the 12531C interface card, except that timing considerations may differ, and the selection of printing or punching by programming means may not apply.

3-4. CHARACTER CODES.

3-5. Teleprinter data is transferred to or from the computer A- or B-register. The data is in the form of 8-bit characters which are placed in, or acquired from, positions 7 through 0 of the register. When punching or reading tape in the teleprinter, these characters can be any 8-bit word. When characters are furnished by the teleprinter keyboard, the character code is modified ASCII (American Standard Code for Information Interchange), with even parity. The parity bit is placed in position 7 of the A- or B-register. (The early version of the 2752A Teleprinter did not have the parity feature. The parity bit is logic 0 if not used.) Characters transferred to the print unit of the teleprinter must use the modified ASCII code.

3-6. TIMING.

3-7. Approximately 0.1 second is required to transfer a character to or from the teleprinter. This period starts at the execution of an STC instruction which initiates the transfer of the character. For a character acquired from the teleprinter keyboard unit, there must be added to the 0.1 second the period of waiting before a key is struck.

3-8. STATUS CHECK.

3-9. Before performing a computer input or output operation involving the teleprinter, the program can check the state of a busy bit acquired from the teleprinter interface card to determine whether the teleprinter is in use. To accomplish this, an LIA or LIB instruction is performed, using the select code of the teleprinter. The sign bit of the word acquired from the interface card is then checked by the program. If this busy bit is logic 1, the teleprinter is sending or receiving a character. If the sign bit is logic 0, the teleprinter is not sending or receiving a character.

3-10. It must be noted, however, that if a series of characters is being transferred, the busy bit becomes logic 0 between each character. The busy bit therefore is used principally for checking the completion of single-character I/O operations. If the teleprinter is set for off-line use or is not turned on, the busy bit is logic 0.

3-11. The busy bit becomes logic 1 during the STC instruction which initiates the transfer of a character to or from the teleprinter. It remains logic 1 until completion of transfer of the character. The busy bit then remains logic 0 until an STC instruction initiates the transfer of another character.

3-12. Table 3-1 shows a typical subroutine which checks the busy bit. The subroutine remains in a waiting loop if the teleprinter is transferring a character.

3-13. CONTROL WORD.

3-14. At the start of each teleprinter I/O operation, a control word is furnished to the teleprinter system to indicate whether an input or output operation is to be performed. In the case of the 2754B Teleprinter, the control word also specifies whether printing, punching, or both are to be performed. (In the 2752A Teleprinter, the punch functions must be selected manually at the teleprinter.) Table 3-2 shows the make-up of the control word, while table 3-3 shows the variations of the control word which can be used with the 2754B Teleprinter.

Table 3-1. Status Check Subroutine

INSTRUCTION	REMARKS
LIA ZZ	This instruction, using the teleprinter select code, loads the busy bit in the sign position of the A-register.
SSA	This instruction causes a skip if the busy bit is logic 0.
JMP *-2	This instruction brings about a program jump back to the LIA instruction.
– – –	From this point the program proceeds to a teleprinter input or output subroutine.

NOTE: ZZ is the teleprinter I/O select code.

Table 3-2. Control Word

BIT	FUNCTION
15	Must be logic 1 to indicate that the word is a control word rather than a data word.
14	Logic 1 to indicate a computer input operation. Logic 0 to indicate an output operation.
13*	Logic 1 to indicate that printing is to be performed.
12*	Logic 1 to indicate that punching is to be performed.
11 thru 0	Perform no function and can be logic 1 or 0.

*In the case of the 2752A Teleprinter these bits perform no function and can be logic 1 or 0.

3-15. PROGRAMMING METHODS.

3-16. As with many other HP input/output devices, programming procedures for the teleprinter can use either the skip-by-flag method or the interrupt method. Skip-by-flag has the advantage that the programming task is simplified; however, the program must remain in a 0.1-second waiting loop for each character transferred.

3-17. The discussion which follows deals first with skip-by-flag programming. Then the interrupt method is covered.

3-18. OUTPUT PROGRAMMING, SKIP-BY-FLAG METHOD.

3-19. Table 3-4 shows a subroutine for printing or punching one character, using the skip-by-flag method. When sending data to the teleprinter by this method, the computer I/O interrupt system must first be turned off; otherwise unwanted teleprinter program-interrupts will occur. The first instruction in table 3-4 turns off the interrupt system.

3-20. Turning off the I/O interrupt system does not disable the power-fail interrupt; nor is the parity-error interrupt or memory-protect interrupt affected, if the optional devices producing these interrupts are installed in the computer.

3-21. After the interrupt system is turned off, an LDA instruction loads the teleprinter control word in the A-register. From the A-register the control word is forwarded to the teleprinter system by an OTA instruction which uses the teleprinter I/O select code. Next, the 8-bit character to be printed or punched is loaded in the low-order end of the A-register by a second LDA instruction. After loading, position 15 of the A-register must contain logic 0 to indicate that a data word, rather than a control word, is being supplied to the teleprinter system. Then an OTA instruction, using the teleprinter I/O select code, transfers the eight bits to the interface card. Finally, an STC instruction with the teleprinter I/O select code initiates the print or punch operation. Approximately 0.1 second is required for the transfer of the character to the teleprinter. The SFS and JMP instructions in table 3-4 keep the routine in a waiting loop until all bits are transferred to the teleprinter. This waiting loop can be omitted if the interrupt system is to remain off.

Table 3-3. Control Words for 2754B Teleprinter

CONTROL WORD (OCTAL)	FUNCTION
110000	Computer output, punch only.
120000	Computer output, print only.
130000	Computer output, print and punch.
140000	Computer input, no printing or punching.
150000	Computer input and punch.
160000	Computer input and print.
170000	Computer input, print and punch.

3-22. The preceding paragraphs described the transfer of a single character to the teleprinter. If more than one

Table 3-4. Skip-by-Flag Output Routine for One Character

INSTRUCTION	FUNCTION
CLF 00	Turn off interrupt system.
LDA XX	Load control word (table 3-2) in A-register.
OTA ZZ	Transfer control word to teleprinter.
LDA YY	Place character in positions 7 through 0 of A-register. Position 15 of the A-register must contain logic 0.
OTA ZZ	Transfer character to teleprinter interface card.
STC ZZ,C	Clear teleprinter interface Flag FF, and start print or punch operation.
SFS ZZ	Check for completion of character transfer to teleprinter.
JMP *-1	If Flag FF is clear (character transfer not complete), return to SFS instruction.
STF 00	Turn on interrupt system.

NOTES: XX is the core-storage location of the control word.
YY is the core-storage location of the character to be printed or punched.
ZZ is the teleprinter I/O select code.

To avoid an unwanted teleprinter interrupt, the interrupt system must not be turned back on until at least 0.1 second after the STC instruction.

character is to be transferred, the control word need not be forwarded again to the teleprinter system. After the first character, the following instructions are required for each additional character:

```
LDA YY
OTA ZZ
STC ZZ,C
SFS ZZ
JMP *-1
```

3-23. The symbols "YY" and "ZZ" above have the same significance as in table 3-4. The SFS and JMP instructions keep the program in a waiting loop for the 0.1-second period required for the transfer of each character to the teleprinter.

3-24. In a multiple-character transfer the I/O routine must include a means of advancing the core-storage address to acquire each successive character. A character count must also be maintained to determine when the I/O operation is complete.

3-25. INPUT PROGRAMMING, SKIP-BY-FLAG METHOD.

3-26. Table 3-5 shows a subroutine for acquiring one character from the teleprinter tape reader unit or keyboard unit. The skip-by-flag method is used, therefore the computer interrupt system must be turned off to avoid unwanted interrupts. The first instruction in table 3-5, CLF 00, performs this function. An LDA instruction then loads the teleprinter control word in the A-register, and an OTA instruction transfers the word to the teleprinter. Next, an STC instruction clears the teleprinter interface Flag FF, and either causes a character to be read from tape (if the teleprinter START/STOP/FREE switch is at the START position), or prepares the system for the striking of a teleprinter key. A waiting loop comprised of an SFS instruction and a JMP instruction awaits the transfer of a character from the teleprinter to the interface card.

Table 3-5. Skip-by-Flag Input Routine for One Character

INSTRUCTION	FUNCTION
CLF 00	Turn off interrupt system.
LDA XX	Load control word (table 3-2) in A-register.
OTA ZZ	Transfer control word to teleprinter system.
STC ZZ,C	Clear teleprinter interface Flag FF, and initiate acquisition of character from teleprinter tape reader unit or await striking of teleprinter key.
SFS ZZ	Check for completion of character transfer to interface card.
JMP *-1	If Flag FF is clear (character transfer not complete), return to SFS instruction.
LIA YY	Flag FF is set. Transfer character from interface card to positions 7 through 0 of A-register. The remainder of the A-register is cleared.
STF 00	Turn on interrupt system.

NOTES: XX is the core-storage location of the control word.
ZZ is the teleprinter I/O select code.
YY is the core-storage location reserved for the character furnished by the teleprinter.

3-27. About 0.1 second is required to transfer a character to the interface card. The teleprinter interface card Flag FF is then set, and an LIA instruction loads the character in the low-order end of the A-register.

3-28. If more than one character is to be acquired from the teleprinter, the control word need not be forwarded again to the teleprinter. After receipt of the first character, the following instructions are required for the acquisition of each additional character:

```
STC ZZ,C
SFS ZZ
JMP *-1
LIA YY
```

3-29. The symbols "ZZ" and "YY" above have the same significance as in table 3-5. The SFS and JMP instructions keep the program in a waiting loop until a character is transferred from punched tape or until a key is struck. When reading from punched tape, the duration of the waiting loop is about 0.1 second. When acquiring a character from the keyboard, the waiting loop continues until about 0.1 second after a key is struck.

3-30. In a multiple-character transfer the I/O routine must include a means of advancing the core-storage address to acquire each successive character. A character count must also be maintained to determine when the I/O operation is complete.

3-31. OUTPUT OR INPUT PROGRAMMING, INTERRUPT METHOD.

3-32. When the interrupt I/O method is used, the I/O routine does not enter a waiting loop while a character is being transferred to or from the teleprinter. Instead, a different subroutine or program is performed during the waiting period. A teleprinter interrupt, occurring at the end of character transfer, brings about a return to the teleprinter I/O routine for completion of the operation.

3-33. The routine for transferring a character to or from the teleprinter is similar to that used for the skip-by-flag method. However, instead of a CLF instruction, an STF instruction with select code 00 (octal) is performed at the start of the routine. This instruction ensures that the interrupt system is turned on.

3-34. For an output operation, the method shown in table 3-6 is used. Table 3-7 shows an input operation.

3-35. In an output operation, if more than one character is to be transferred the following instructions are required for each additional character:

LDA YY
OTA ZZ
STC ZZ,C
JMP

3-36. For a multiple-character input operation, each additonal character requires the following:

STC ZZ,C
JMP
LIA ZZ (When a teleprinter interrupt occurs)
STA YY

3-37. The program or routine performed while awaiting an interrupt must not initiate a different teleprinter operation.

Table 3-6. Interrupt-Method Output Routine

INSTRUCTION	FUNCTION
STF 00	Ensure that the interrupt system is turned on.
LDA XX	Load control word (table 3-2) in A-register.
OTA ZZ	Transfer control word to teleprinter.
LDA YY	Place character in positions 7 through 0 of A-register. Position 15 of the A-register must contain logic 0.
OTA ZZ	Transfer character to teleprinter interface card.
STC ZZ,C	Clear teleprinter interface Flag FF, and start print or punch operation.
JMP	Jump to a different subroutine of program.
NOTES: When a teleprinter interrupt occurs, a JSB instruction produces a program jump to the routine for transferring the next character (if any) to the teleprinter. XX is the core-storage location of the control word. ZZ is the teleprinter I/O select code. YY is the core-storage location of the character to be printed or punched.	

Table 3-7. Interrupt-Method Input Routine

INSTRUCTION	FUNCTION
STF 00	Ensure that the interrupt system is turned on.
LDA XX	Load control word (table 3-2) in A-register.
OTA ZZ	Transfer control word to teleprinter.
STC ZZ,C	Clear teleprinter interface Flag FF, and initiate acquisition of character from teleprinter tape reader unit or await striking of teleprinter key.
JMP	Jump to a different subroutine or program.
When a teleprinter interrupt occurs, a JSB instruction produces a program jump to the remainder of the teleprinter I/O subroutine, below.	
LIA ZZ	Transfer character from interface card to positions 7 through 0 of A-register. The remainder of the A-register is cleared.
STA YY	Store the character.
NOTES: XX is the core-storage location of the control word. ZZ is the teleprinter I/O select code. YY is the core-storage location reserved for the character furnished by the teleprinter.	

3-38. PARITY CHECKING.

3-39. INPUT.

3-40. Characters supplied by keys actuated at the teleprinter keyboard have a parity bit; even parity is used. (The early version of the 2752A Teleprinter did not have this feature.) Characters from punched tape have a parity bit if the tape was produced with this bit. In both cases, the parity bit is one of the eight bits provided, and in the case of a keyboard character it is placed in position 7 of the A- or B-register. No hardware check is made of the parity bit; but it can be checked by programming means, if desired.

3-41. OUTPUT.

3-42. No hardware check is made of parity bits furnished to the print unit or punch unit, nor is it possible to determine directly by programming means whether a parity error has occurred. In the case of punched tape, however, the tape can later be read and checked by a programmed parity test or by a comparison with the original data. If a parity bit is used with punched tape, a routine must determine whether logic 1 or 0 is required, and must establish the required bit in the 8-bit character. (That is, these functions are not performed by hardware.)

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section explains the circuit theory of the buffered teleprinter interface card. The discussion concerns mainly teleprinter operations, but it is also applicable to use of the interface card with other types of I/O devices. Signal timing for other I/O devices may differ from teleprinter timing; and some I/O devices may use only a single stop bit, rather than the two used by the teleprinter.

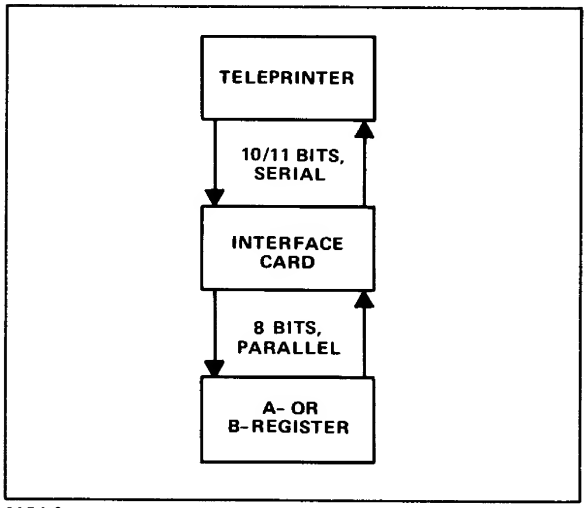
4-3. The term "input" in this section signifies data input to the computer, while "output" indicates output from the computer. Mention of the "keyboard", the "punch unit", and the "tape reader" refer to these units in the teleprinter.

4-4. Before starting the circuit theory discussion which follows, the reader should be familiar with the programming information provided in Section III of this manual.

4-5. During the theory discussion, reference should be made as required to figure 5-2, the logic diagram of the interface card.

4-6. DATA TRANSFER.

4-7. It has been noted that data is transferred to and from the teleprinter in the form of 8-bit words. These words are transferred in parallel between the A- or B-register and the interface card (figure 4-1). In an output operation the word is stored temporarily in a register on the interface card, and three bits are added to it. These are a start bit (logic 0), and two stop bits (logic 1's). The 11 bits



2154-8

Figure 4-1. Bit Transfer Method

are then transferred serially to the teleprinter, commencing with the start bit, and ending with the two stop bits (figure 4-2).

4-8. In a teleprinter input operation, an 11-bit word is received by the interface card for each key struck or for each group of eight holes read from punched tape. The 11 bits are transferred serially to the register on the interface card. As in an output operation, the eight data bits are preceded by a start bit, and followed by two stop bits. At the interface card the start and stop bits are discarded, and the eight data bits are transferred in parallel from a register on the interface card to the A- or B-register. The upper waveform in the illustration appears at pins 16 and T of the interface card 48-pin connector when an "S" is transferred to the teleprinter. The lower waveform appears at pins 4 and D when an "S" is received from the teleprinter.

4-9. For the teleprinter, the serial transfer of each bit of an 11-bit word requires approximately 9.09 milliseconds. The entire 11 bits are transferred in about 0.1 second. The parallel transfer of 8-bit words between the interface card and the A- or B-register is completed within one computer machine cycle. Data transfer times are the same for input and output.

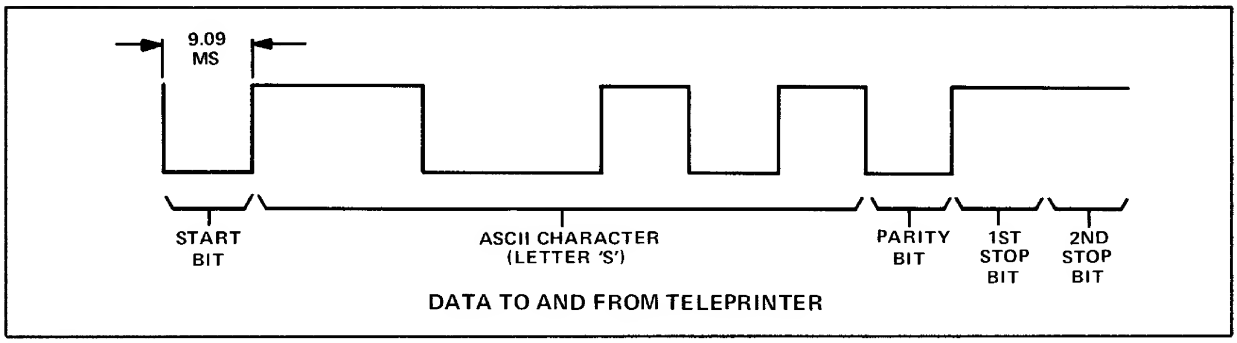
4-10. POWER-ON AND PRESET-SWITCH FUNCTIONS.

4-11. When power is initially applied to the computer, the interface card receives a POPIO(B) (Power On Pulse to I/O, Buffered) signal and a CRS (Control Reset to I/O) signal. (See figure 4-10.) Both signals consist of a train of T5 pulses, lasting for approximately 40 milliseconds during the power turn-on period. The POPIO(B) signal sets the Flag Buffer FF. The CRS signal clears the Control FF, the Clock Enable FF, the Print FF, the Punch FF, and the Read FF. Frequency Divider B is also cleared, and the In/Out FF is set.

4-12. When the Clock Enable FF is cleared by the CRS pulse, the set-side output of the flip-flop clears flip-flop U85A in the data register, and sets flip-flop U85B.

4-13. With the Print and Punch FFs in the clear condition, transistor Q4 is cut off, and the data line to the teleprinter is maintained at the logic 1 level.

4-14. An additional function during power turn-on is the setting of the Flag FF, and the clearing of the IRQ (Interrupt Request) FF. These actions are brought about by the ENF (Enable Flag) signal. The first of the ENF pulses clears the IRQ FF. Then, when the Flag Buffer FF is set by the POPIO pulse, the Flag FF is likewise placed in the set condition.



2154-7A

Figure 4-2. Data Waveforms (Typical) To and From Teleprinter

4-15. Summarizing the state of the interface card after power turn-on, the following conditions exist:

a. The Flag Buffer FF, the In/Out FF, flip-flop U85B in the data register, and the Flag FF are set.

b. Frequency divider B is cleared.

c. The Control FF, the Clock Enable FF, the Print FF, the Punch FF, the Read FF, flip-flop U85A in the data register, and the IRQ FF are in the clear condition.

d. The output data line to the teleprinter is at the logic 1 level.

4-16. Whenever power is applied to the computer and a program is not running, pressing the PRESET switch produces manually the same effects that occur during power turn-on.

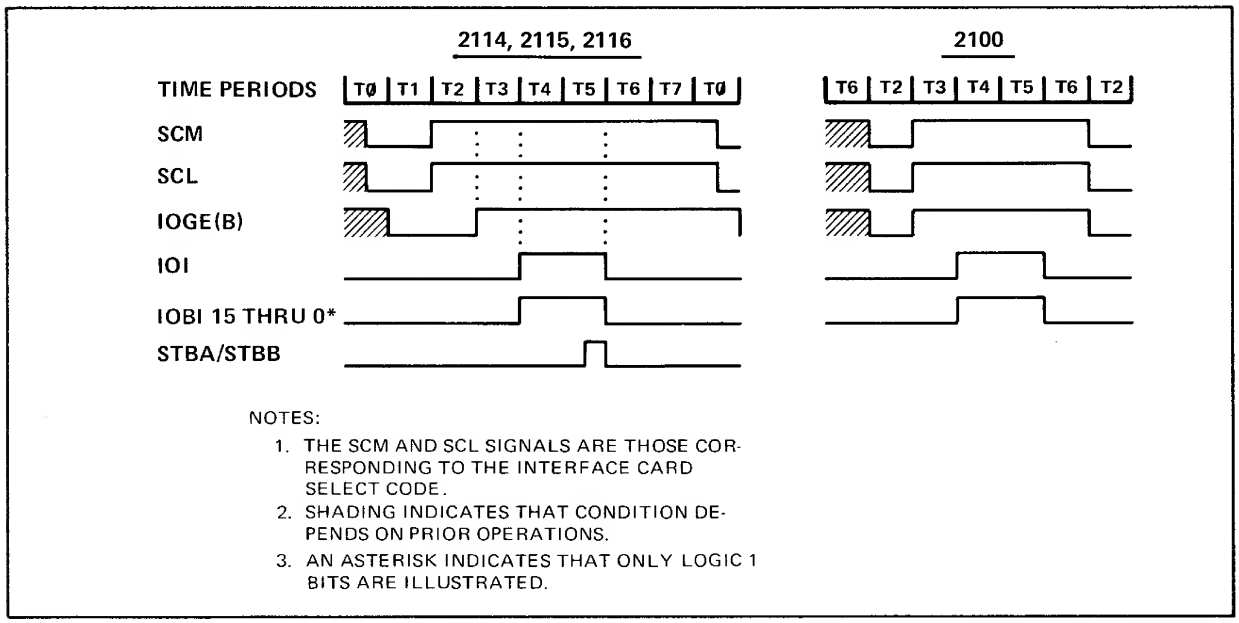
4-17. STATUS CHECK.

4-18. When an LIA or LIB instruction is performed to make a teleprinter status check, bit 15 of the A- or B-register is loaded from the IOBI 15 line. When the teleprinter is busy, the Clock Enable FF on the interface card is set, and the bit is logic 1. When the teleprinter is not busy, the flip-flop is clear, and the bit furnished is logic 0.

4-19. Timing relationships of signals generated by the LIA/B instruction are illustrated in figure 4-3. The STBA/STBB signal in the illustration is not furnished to the interface card; the signal loads the status bit into the A- or B-register.

4-20. INPUT OPERATION.

4-21. The paragraphs which follow describe a computer input operation. During the discussion, reference should be made as required to the flow chart in figure 4-11.



2154-2A

Figure 4-3. LIA/B Instruction, Timing Chart

4-22. OTA/B INSTRUCTION.

4-23. To prepare for an input operation, an OTA/B instruction transfers a control word to the interface card. Figure 4-4 illustrates the signals furnished to the card when the instruction is performed, and table 3-2 shows the format of the control word. To indicate an input operation, bit 14 of the control word is logic 1. As a result the In/Out FF is set, and this flip-flop brings about the following:

a. Enables gate U94C, permitting a clock pulse to be supplied to the Data Register FFs when the C FF becomes set.

b. Enables gate U34A, permitting the setting of the Clock Enable FF when the start bit is received from the teleprinter.

c. Enables gate U24B, permitting data received from the teleprinter to be returned to the teleprinter for printing or punching if the Print or Punch FF is set.

4-24. The IOO signal results in the clearing of flip-flop U95B and seven additional flip-flops in the data register. Flip-flop U124B in the register is set; the logic 1 from this flip-flop is later shifted down the register to flip-flop U85B, where it remains until the next teleprinter operation. This logic 1 maintains the logic 1 level required on the data line to the teleprinter when the teleprinter is not in use.

4-25. If characters furnished by the teleprinter are to be printed or punched by the teleprinter itself, the Print FF or Punch FF is set by the appropriate bit of control word. With the 2752A Teleprinter it is also necessary that manual controls on the teleprinter be set for the required function (print or punch).

4-26. STC INSTRUCTION.

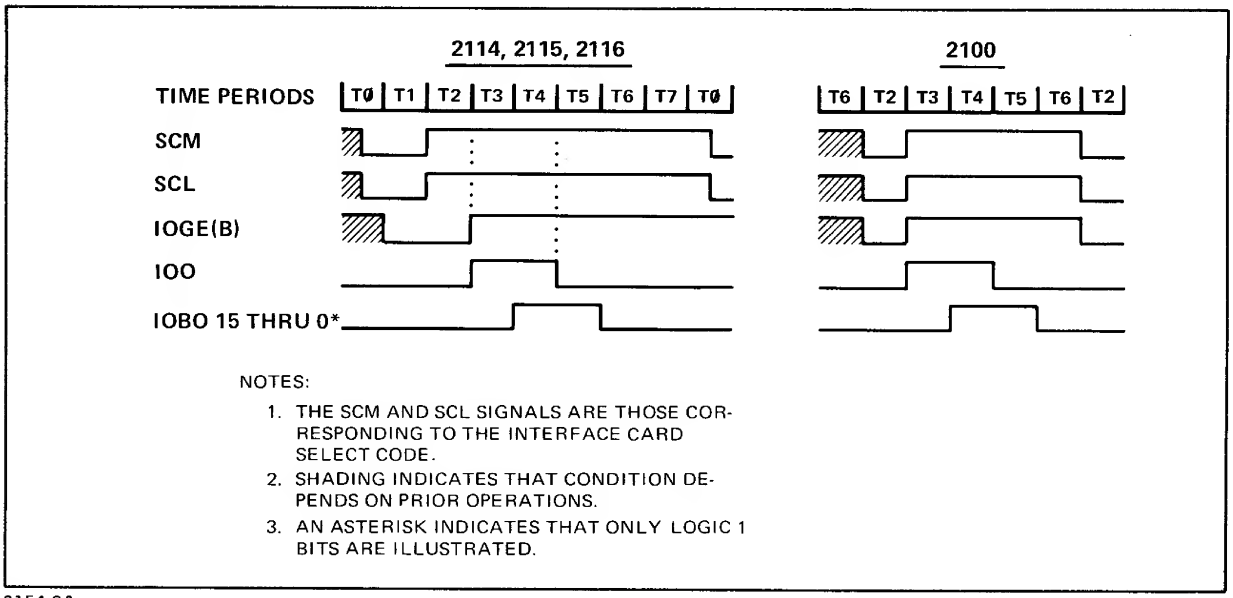
4-27. An STC instruction (figure 4-5) starts the transfer of a character from the teleprinter tape reader, or prepares for the receipt of characters from the keyboard. The H/C bit (hold/clear Flag FF bit) of the instruction word is logic 1. Consequently, the CLF signal becomes true at time T4, and the Flag Buffer FF and Flag FF are cleared.

4-28. The STC signal becomes true at T4, and the Control FF is set. If the I/O interrupt system is on, the set condition of the Control FF allows the IRQ FF to be set when a character has been transferred from the teleprinter to the data register on the interface card. With the IRQ FF set, a teleprinter interrupt occurs. If a skip-by-flag I/O operation is being performed, the Control FF and IRQ FF perform no useful function.

4-29. The STC signal also sets the Read FF. As a result, a Read Command signal is sent to the teleprinter. If the teleprinter tape reader is turned on, a set of eight holes is read from punched tape. If the tape reader is not turned on, operations await the striking of a key on the teleprinter keyboard. (The tape reader is turned on when the FREE/STOP/RUN switch on the 2754B Teleprinter is at the RUN position, or when the START/STOP/FREE switch on the 2752A Teleprinter is at the START position.)

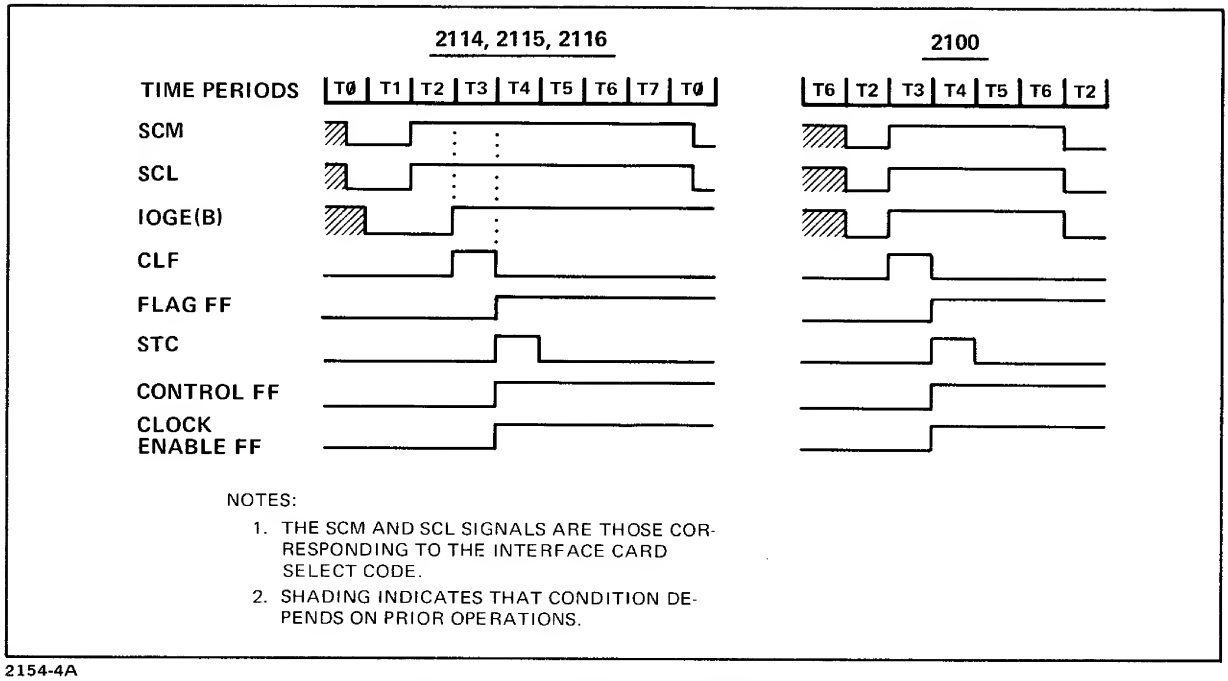
4-30. DATA TRANSFER.

4-31. After the STC instruction initiates the transfer of a character from the teleprinter, the computer either enters a waiting loop (for a skip-by-flag operation) or proceeds with another program or routine (in the case of an interrupt-type I/O operation).



2154-3A

Figure 4-4. OTA/B Instruction, Timing Chart



2154-4A

Figure 4-5. STC Instruction, Timing Chart

4-32. At the teleprinter, data transfer to the interface card commences when the tape reader reads a character or when a key on the keyboard is struck. As noted earlier, for each character 11 bits are transferred from the teleprinter to the interface card. These are furnished to pins 4 and D of the 48-pin connector on the card.

4-33. The data pulses are applied to a Schmitt trigger (Q1, Q2), which shapes the leading edges of the pulses. Transistor Q3 converts the Schmitt trigger output to the required voltage levels.

4-34. The start bit turns on the Clock Enable FF. Then, if jumper wire W1 is connected to terminal A (which is the case for teleprinter use), the clock pulses produced by frequency divider A are furnished to frequency divider B. If an external clock pulse is used, W1 is connected to terminal B, and frequency divider B receives externally produced clock pulses.

4-35. In the case of the teleprinter, jumper wire W2 is installed. Jumper W2 provides for a bit transfer rate of 110 bits per second. At this bit rate, the C FF in frequency divider B is set 4.545 milliseconds after the Clock Enable FF permits frequency divider B to commence operation. When set, the C FF furnishes a shift pulse to the data register flip-flops, and the start bit is shifted into flip-flop U124B. The 4.545-millisecond delay before the start bit is sampled eliminates problems arising from contact bounce. Every 9.09 milliseconds thereafter, another shift pulse is furnished to the data register flip-flops, and a new bit is shifted into the data register. Bits previously in the register are moved down the register one position each time a new bit is placed in flip-flop U124B. As with the start bit, each bit is sampled at the center of the data pulse. Figure 4-6 shows the timing relationships.

4-36. After 10 shifts, the start bit is in flip-flop U85A of the data register, the eight character-bits are in the flip-flops shown above U85A in the logic diagram, and the first stop bit is in flip-flop U124B. At this time the Counter Reset FF is cleared, and frequency divider B ceases functioning. As a result, no further shift pulses are supplied to the data register, and when the second stop bit is furnished by the teleprinter, it is not loaded into the register.

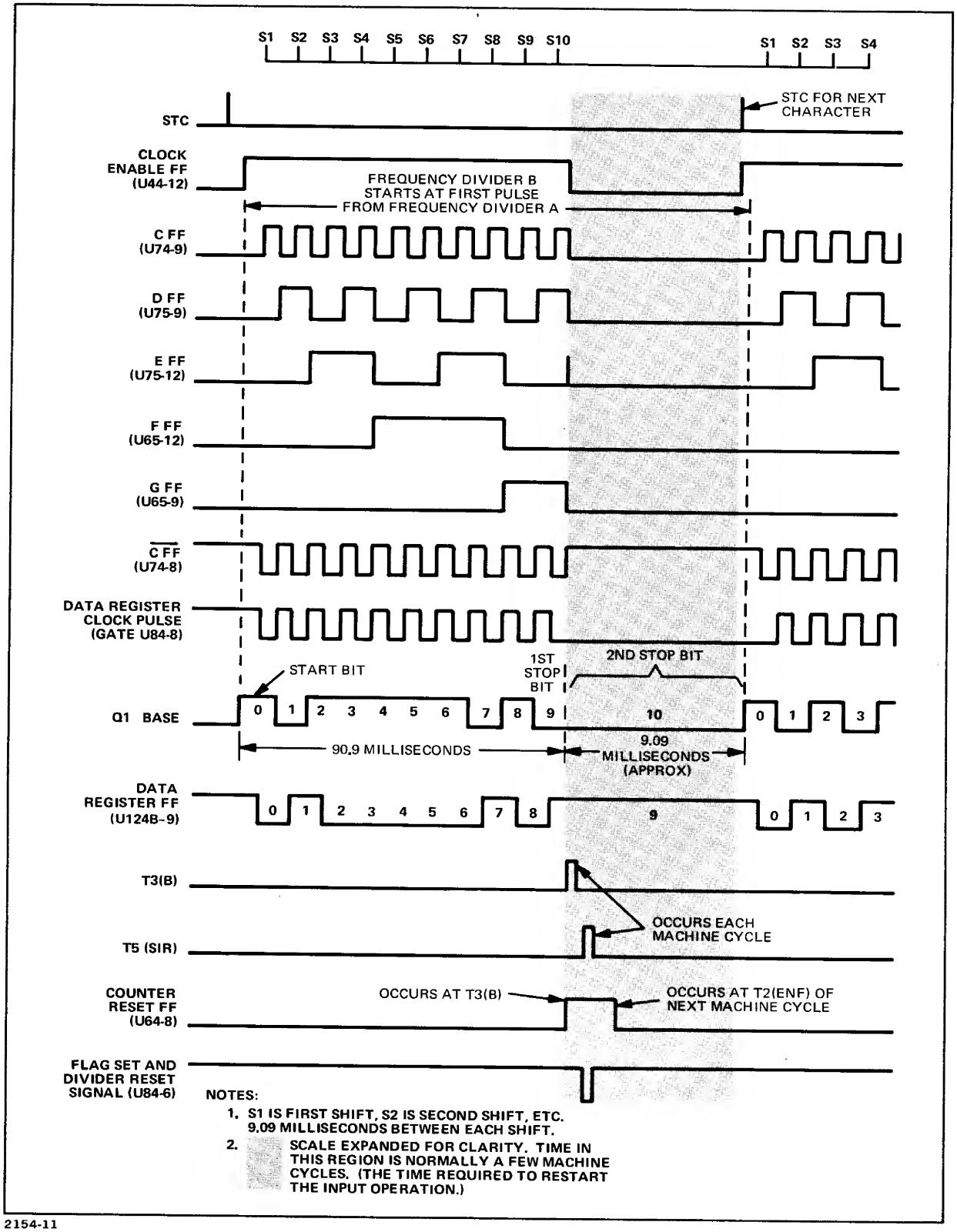
4-37. When frequency divider B is cleared, the Flag Buffer FF is set. This is followed by the setting of the Flag FF.

4-38. If a skip-by-flag I/O operation is being performed, the next execution of an SFS instruction results in the SKF signal becoming true (figure 4-7). A program skip then occurs.

4-39. If an interrupt-type I/O operation is being performed, the I/O interrupt system is on, and the IEN signal is true. If the PRH signal also is true, the IRQ FF is set. The true IRQ and FLG signals bring about a program interrupt.

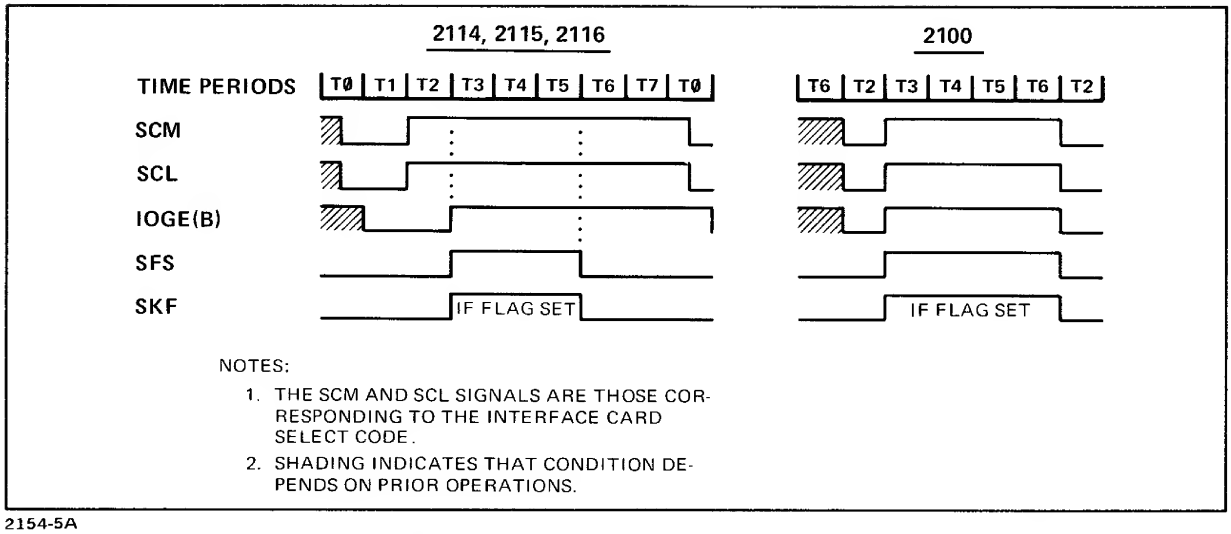
4-40. LIA/B INSTRUCTION.

4-41. An LIA/B instruction transfers the character from the data register on the interface card to the A- or B-register. The instruction strobes the gates at the outputs of the data register flip-flops, and the 8-bit character in the register is gated onto the IOBI-0 through IOBI-7 lines.



2154-11

Figure 4-6. Computer Input Operation (Teleprinter), Timing Chart



2154-5A

Figure 4-7. SFS Instruction, Timing Chart

From there, the character bits are gated into positions 0 through 7 of the A- or B-register. At this time the Clock Enable FF is clear, and logic 0 is gated into position 15 of the A- or B-register. The remaining positions of the A- or B-register are cleared.

4-42. OUTPUT OPERATION.

4-43. The paragraphs which follow describe a computer output operation. During the discussion, reference should be made as required to figure 4-12.

4-44. FIRST OTA/B INSTRUCTION.

4-45. In an output operation, an OTA/B instruction transfers a control word to the interface card. The functions of the control word are the same as for an input operation, except that the In/Out FF is cleared, rather than set. This results from the fact that bit 14 of the control word is logic 0. In the clear condition, the In/Out FF brings about the following:

a. Enables gate U34D, permitting the Clock Enable FF to be set when an STC instruction initiates the transfer of a character to the teleprinter.

b. Enables gate U94A, permitting a shift pulse to be sent to the data register each time the C FF is cleared.

c. Enables gate U55B, allowing frequency divider B to be stopped after 11 bits have been supplied to the teleprinter.

d. Enables gate U24C, permitting data to be forwarded from the data register to the teleprinter.

4-46. SECOND OTA/B INSTRUCTION.

4-47. After the control word has been furnished to the interface card, an OTA or OTB instruction forwards the 8-bit data word to the card. The bits are furnished on the IOBO-0 through IOBO-7 lines, and are placed in the data register. Prior to this, flip-flop U124B of the data register is set by a false input to its direct clear terminal, pin 10.

4-48. STC INSTRUCTION.

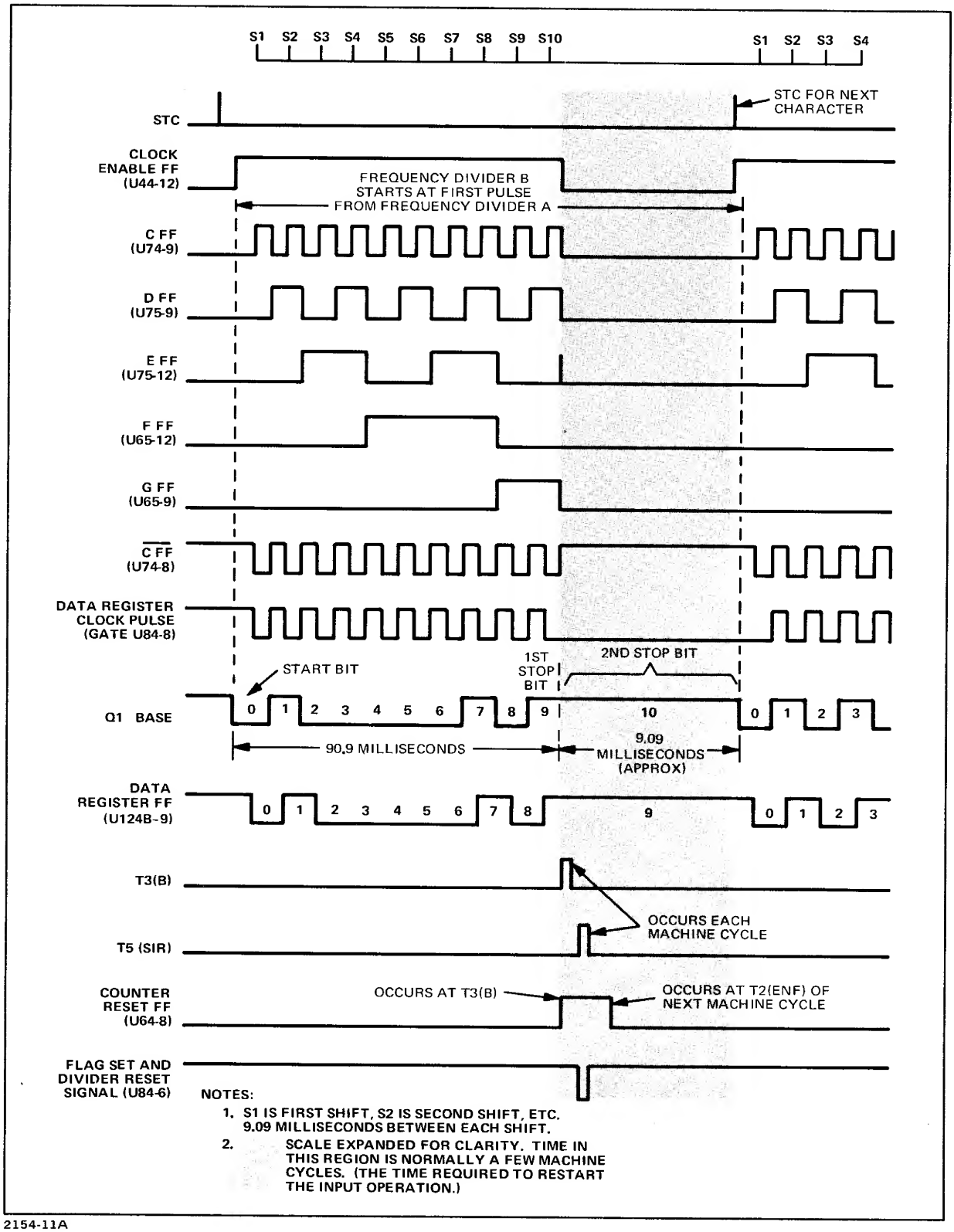
4-49. Following the loading of the data register on the interface card, an STC instruction is performed. This instruction clears the Flag Buffer FF and the Flag FF, and sets the Control FF and Clock Enable FF.

4-50. It has been seen that in an input operation the Clock Enable FF is set when a start bit is received from the teleprinter. In the output operation presently under discussion, this flip-flop is set as soon as the STC instruction initiates data transfer operations.

4-51. DATA TRANSFER.

4-52. With the Clock Enable FF set, frequency divider B starts operating (figure 4-8). Previously, flip-flop U85B in the data register was set and U85A was cleared by the set-side output of the Clock Enable FF. With U85B set, the data line to the teleprinter (pins 16 and T of the 48-pin connector) is true. When frequency divider B has been operating for 4.545 milliseconds, the C FF is set. After another 4.545 milliseconds, the C FF is cleared. At this time a shift pulse is furnished to the data register, and the logic 0 in flip-flop U85A is shifted into U85B. The other bits in the data register also are shifted downward one position in the register. When U85B receives the logic 0, the data line to the teleprinter becomes false. This false level is the start bit for the teleprinter, and mechanical functions in the teleprinter commence. Each 9.09 milliseconds thereafter the C FF is cleared, and a new bit is furnished to the teleprinter.

4-53. When the contents of the data register have been shifted for the eleventh time, the 11 bits initially in the



2154-11A

Figure 4-8. Computer Output Operation (Teleprinter), Timing Chart

data register have all been transferred to the teleprinter. The last two bits are the stop bits. The first of these results from the setting of flip-flop U124B of the data register by the OTA/B instruction which loaded the register. The second stop bit results from the fact that U124B remains in the set condition after the first shift. (In effect, a logic 1 is placed in U124B each time a shift takes place because the output of gate U104C is true.)

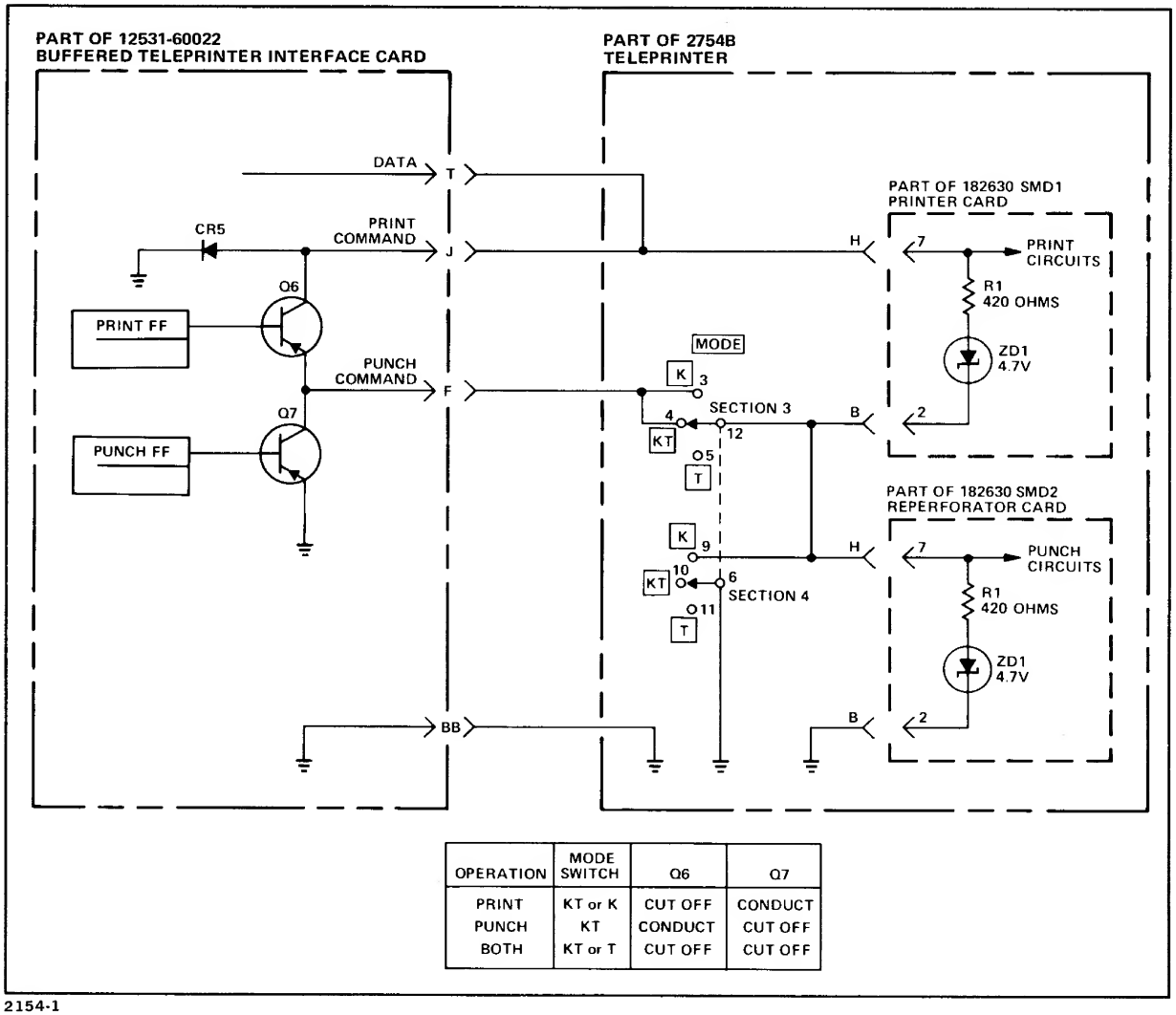
4-54. At the eleventh shift, frequency divider B is cleared and the Flag Buffer FF is set. Shortly thereafter the Flag FF is set. A program skip then occurs (for a skip-by-flag operation) or an interrupt takes place.

4-55. PRINT AND PUNCH CONTROL CIRCUITS.

4-56. Figure 4-9 illustrates the circuits which permit program selection of printing or punching in the 12754B Teleprinter. (As pointed out earlier, the 2752A Teleprinter requires manual selection of these functions.) The Print FF is set for printing, and the Punch FF is set for punching. The flip-flops are placed in the desired state by the control word which is sent to the interface card before the start of data transfer.

4-57. In a print-only operation, the Punch FF is clear and the Print FF is set. Consequently, transistor Q7 conducts heavily and Q6 is cut off. When data transfer begins, the data bits are developed across resistor R1 and diode ZD1 of the SMD1 printer card. Pin 2 of this card is maintained at close to ground potential because Q7 is conducting. No voltage is developed across R1 and ZD1 of the SMD2 reperforator card because Q7 shorts the input to the card.

4-58. When a punch-only operation is performed, Q6 conducts heavily and Q7 is cut off. As a result, the data signal passes through Q6 and is developed in the SMD2 card only. When printing and punching are conducted simul-



OPERATION	MODE SWITCH	Q6	Q7
PRINT	KT or K	CUT OFF	CONDUCT
PUNCH	KT	CONDUCT	CUT OFF
BOTH	KT or T	CUT OFF	CUT OFF

2154-1

Figure 4-9. 2754B Teleprinter Print and Punch Control Circuits, Simplified Schematic Diagram

taneously, Q6 and Q7 are both cut off. Consequently, half the signal voltage is developed in the SMD1 card, and half in the SMD2 card. The circuits are designed to function normally on this half voltage.

4-59. Diode CR5 prevents damage to Q6 and Q7 in the event that the 48-pin connector for the interface card is removed while the computer is turned on. If the ground pins in the connector break contact before the pins carrying the print command and punch command signals, excessive voltage is applied to the collector or Q6. This high voltage would destroy Q6 and Q7 if not bypassed by CR5.

CAUTION

Regardless of the protective function of diode CR5, always turn off computer power before removing the 48-pin connector. The diode itself could be defective, eliminating protection.

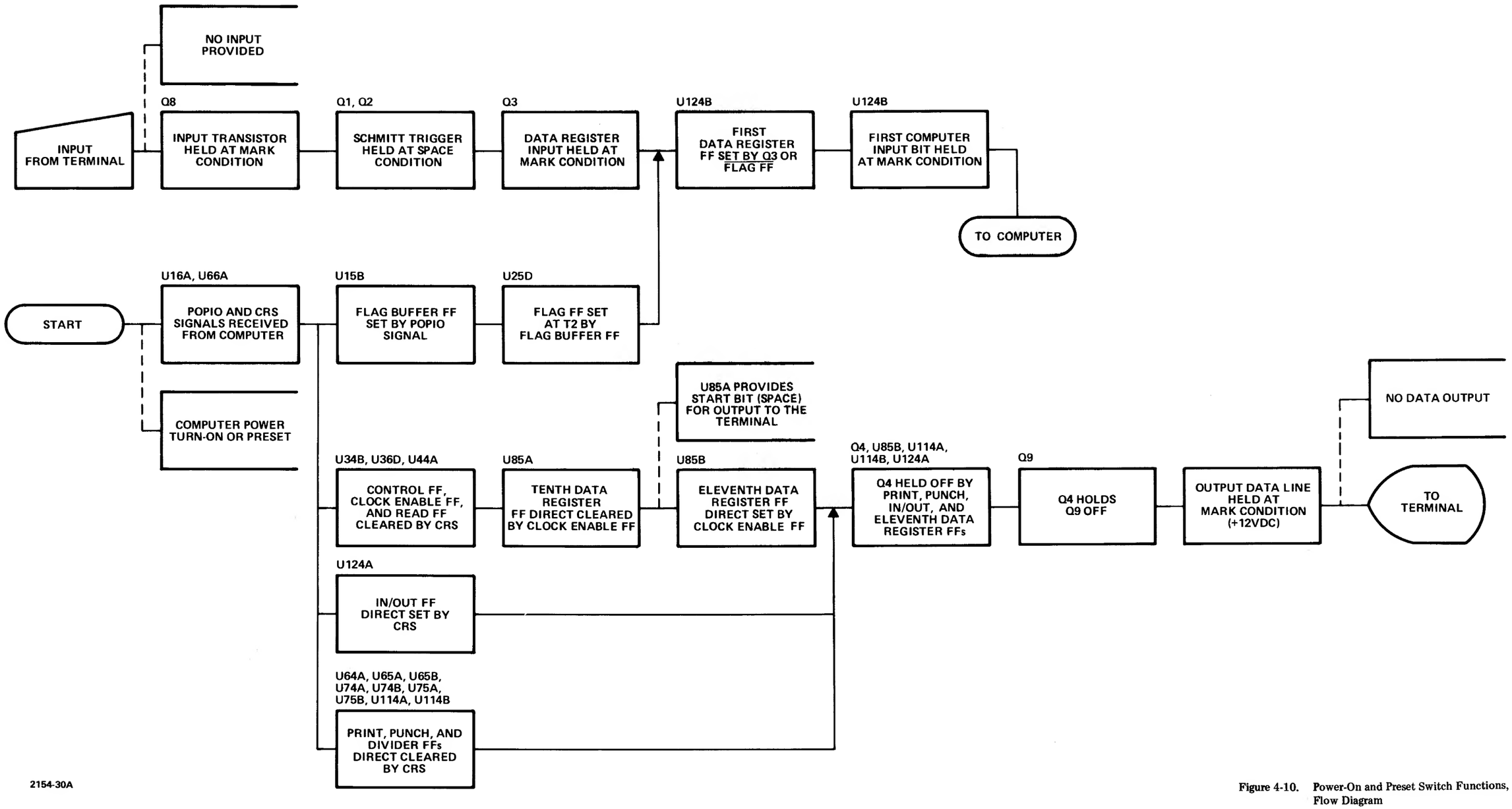
4-60. EIA COMPATIBLE DEVICE OPERATION.

4-61. The interface card can be used with a Bell series 103A Data-Phone (or other terminals such as the HP 2749A or 2600A) instead of a teleprinter. As with the teleprinter, characters transferred to the devices each consist of 11 bits, including a start bit and two stop bits. Characters from these devices may be 10 or 11 bits depending on whether one or two stop bits are supplied. However, the data waveforms entering and leaving the interface card are inverted from those associated with the teleprinter. Therefore, the waveforms shown in figure 4-2 must be inverted for Data-Phone application.

4-62. As well as being inverted, the signal waveforms for the Data-Phone have different levels from the teleprinter signals. Table 1-1 specifies these levels.

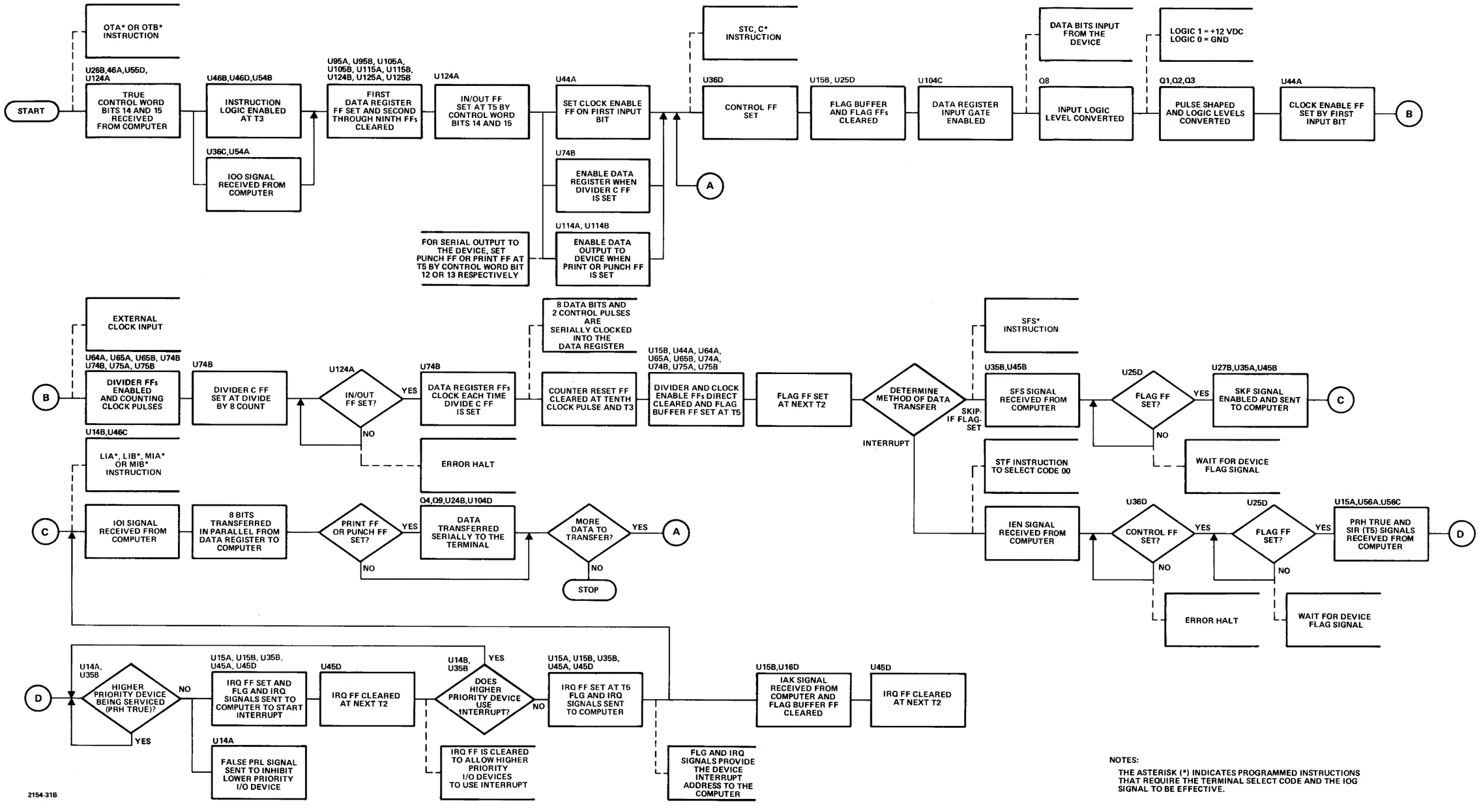
4-63. Data bits from these devices are applied to pin X on the interface card. Transistor Q8 inverts the signal and changes its voltage levels to correspond to those from the teleprinter. The 48-pin plug used on the interface card has a jumper connecting pin Y with pins 4 and D. Thus, after inverting and level shifting, the signal is applied to the circuit card as if it were from the teleprinter.

4-64. Output data signals leave the interface card from pins 16 and T of the 48-pin connector. A jumper connects these pins to pin V. The level is changed and the signal is inverted by transistor Q9. Pin W transfers the outgoing signal to the I/O device. Pins 17 and U furnish +12 volts for use by the Data-Phone or terminal.



2154-30A

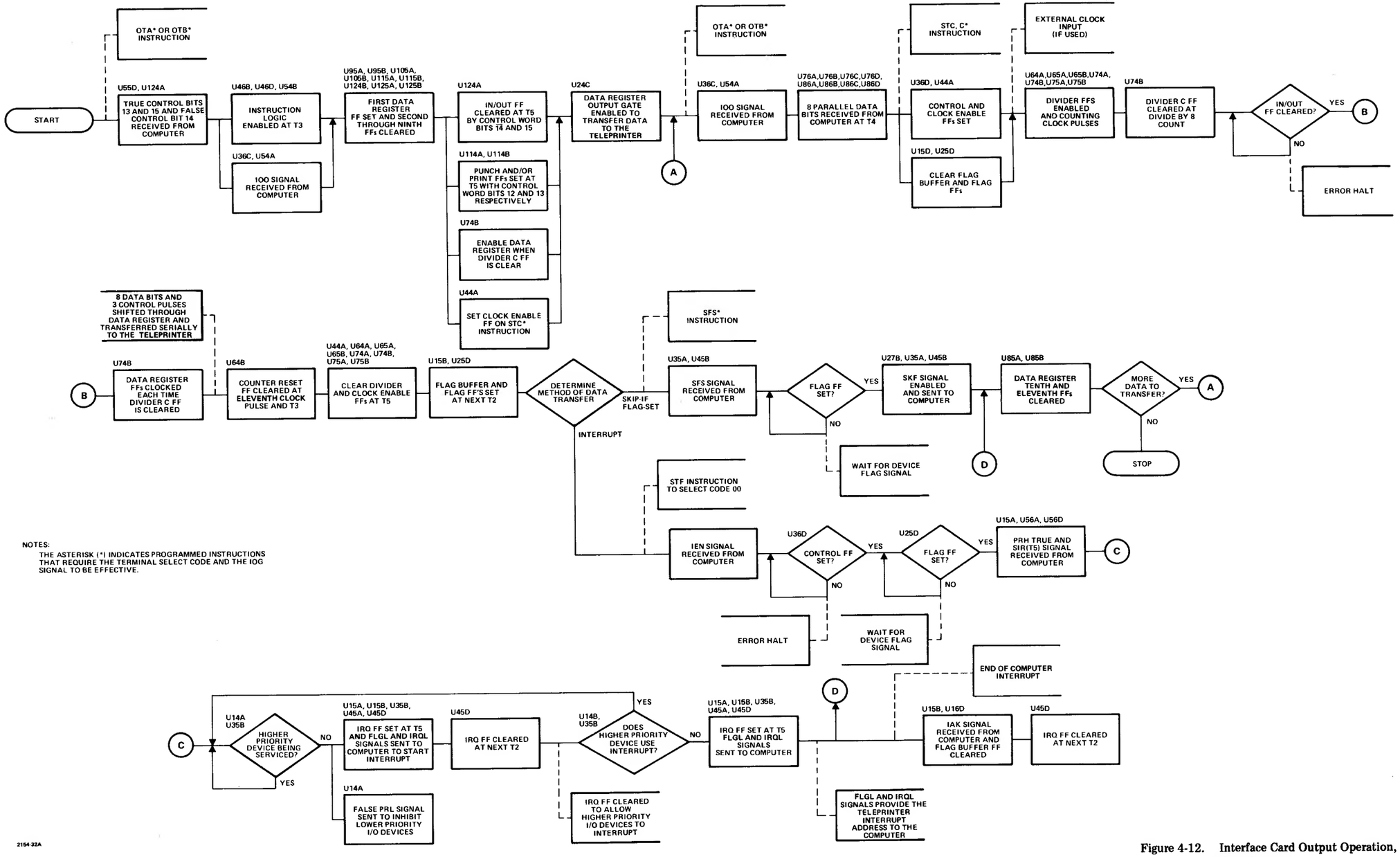
Figure 4-10. Power-On and Preset Switch Functions, Flow Diagram



NOTES:

THE ASTERISK (*) INDICATES PROGRAMMED INSTRUCTIONS THAT REQUIRE THE TERMINAL SELECT CODE AND THE IOG SIGNAL TO BE EFFECTIVE.

Figure 4-11. Interface Card Input Operation, Flow Diagram



NOTES:

THE ASTERISK (*) INDICATES PROGRAMMED INSTRUCTIONS THAT REQUIRE THE TERMINAL SELECT CODE AND THE IOG SIGNAL TO BE EFFECTIVE.

2154-32A

Figure 4-12. Interface Card Output Operation, Flow Diagram

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides maintenance information for the 12531-60022 Buffered Teleprinter Interface Card. Included are corrective maintenance instructions and reference data for troubleshooting. Tables and diagrams presented in this section are arranged in the following order:

a. Sample I/O test programs (table 5-1).
b. Connections to 2752A Teleprinter (table 5-2).
c. Connections to 2754B Teleprinter (table 5-3).
d. Interface card replaceable parts list (table 5-4).
e. Integrated circuit pin connections and characteristics (figure 5-1).
f. Interface card parts location and logic diagram (figure 5-2).

5-3. PREVENTIVE MAINTENANCE.

5-4. Preventive maintenance for the interface kit is performed at the same intervals as for the computer system as a whole.

5-5. Preventive maintenance consists of inspecting the interface card for burned or broken components, or the presence of foreign material. The cable and connector which attach to the front of the card should also be checked for damaged insulation, bent or broken pins, etc. After any damage has been repaired, run the off-line diagnostic program (if any) for the I/O device. (The applicable off-line diagnostic program is specified in the operating and service manual for the device.) Finally, run an on-line diagnostic program to check the interface card with the I/O device connected. For the teleprinter, use the on-line diagnostics designated in paragraph 2-18. Procedures for running diagnostic programs are described in the *Manual of Diagnostics*.

5-6. CORRECTIVE MAINTENANCE.

5-7. GENERAL.

5-8. Most malfunctions of the interface card can be traced by performing the teleprinter diagnostic program and analyzing error halts as they occur. Oscilloscope checks facilitate localizing the fault to a component.

5-9. When performing troubleshooting, refer to figures 5-1 and 5-2. Table 5-1 contains sample programs for testing data transfer between the computer and the I/O device. Connections to the interface card 48-pin connector are listed in tables 5-2 and 5-3. Parts information is provided in table 5-4. For connections to the 86-pin connector, refer to the computer installation and maintenance manual.

5-10. SIGNAL VOLTAGES.

5-11. The voltages of teleprinter signals entering and leaving the interface card are listed in table 1-1.

5-12. For voltage levels of signals received by the interface card from the computer, refer to the computer installation and maintenance manual.

5-13. To determine the input voltages, output voltages, and circuit delay of integrated circuits on the interface card, first find the integrated circuit diagram in figure 5-1. Then refer to the appropriate characteristic at the bottom of the figure.

Table 5-1. Sample Input/Output Test Programs

Input Program

```
40   CLC   00     Turn off I/O interrupt system
     LDA   71     Load A-register with control word
     OTA   SC     Output control word
     STC   SC,C   Set control, clear flag
     SFS   SC     Wait for flag
     JMP   *-1
     LIB   SC     Input data word
     OTB   01     Output data word (000101₈)
                  to Switch Register (2114 and
                  2100 Computers only)
     JMP   40     Return for next data word
71   160000       Control word
```

Output Program

Set the Switch Register to 123202_8

```
20   CLC   00     Turn off I/O interrupt system
     LIA   01     Load data from Switch Register
     OTA   SC     Output data word
     STC   SC,C   Set control, clear flag
     SFS   SC     Wait for flag
     JMP   *-1
     JMP   20     Return for next output
```

Table 5-2. Connections to 2752A Teleprinter

INTERFACE CARD PIN	WIRE COLOR	TELEPRINTER CONNECTION*	SIGNAL
4,D	Black	Pin 3 of teleprinter rear connector	Computer input data
12,N	Red	+12 volt input on card assembly** (one end of resistor R1)	+12 volts
14,R	White-brown	-12 volt input on card assembly** (one end of resistor R3)	-12 volts
16,T	Green-orange	Pin 7 of teleprinter rear connector	Computer output data
13,P	Yellow	Read command input to card assembly** (junction of resistors R1 and R2)	Read command
24,BB	Cable shield	Ground connection on card assembly** (emitter of transistor Q2)	Ground

NOTES: *Refer to the schematic diagram in the HP 2752A Teleprinter manual for components specified in this table.
**"Card assembly" refers to the printed circuit card added during modification of the Teletype Corporation Model ASR-33 Teletypewriter Set.

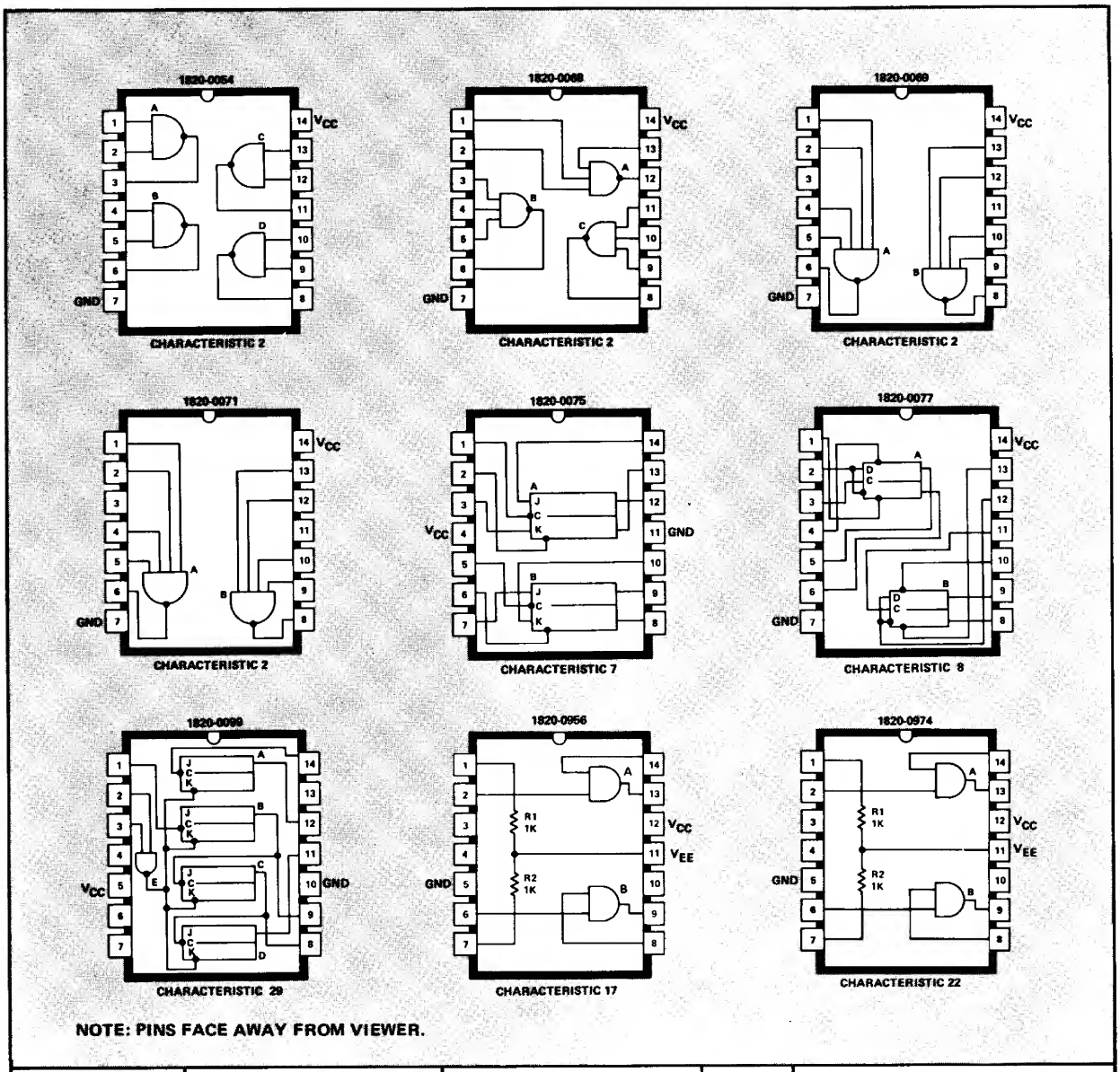
Table 5-3. Connections to 2754B Teleprinter

INTERFACE CARD PIN	WIRE COLOR	TELEPRINTER CONNECTION*	SIGNAL
4,D	Black	Terminal T6	Computer input data
12,N	Red	+12 volt input on card assembly** (one end of resistor R1)	+12 volts
14,R	Brown	-12 volt input on card assembly** (one end of resistor R3)	-12 volts
16,T	White	Terminal T7	Computer output data
13,P	Yellow	Read command input to card assembly** (junction of resistors R1 and R2)	Read command
24,BB	White, black, & cable shield	Ground connection on card assembly** (emitter of transistor Q2)	Ground
6,F	Orange	Terminal T8	Punch Control
8,J	Green	Terminal T4	Print Control

NOTES: *Refer to the schematic diagram in the HP 2754B Teleprinter manual for components specified in this table.
**"Card assembly" refers to the printed circuit card added during modification of the Teletype Corporation Model ASR-35 Teletypewriter Set.

Table 5-4. Buffered Teleprinter Interface Card, Replaceable Parts List

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0160-0263	Capacitor, Fxd, Cer, 0.22 uF, 20%, 50 VDCW	56289	5C52BS-CML
C2	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	56289	192P10292-PTS
C4	0160-2940	Capacitor, Fxd, Mica, 470 pF, 5%, 300 VDCW	72136	RMD15F471J3C
C5	0140-0191	Capacitor, Fxd, Dipped Mica, 56 pf, 5%	28480	0140-0191
C8, 10, 12 thru 24	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X9035A2
C9	0180-0338	Capacitor, Fxd, Elect, 25 uF, +75 -10%, 25 VDCW	28480	0180-0338
CR1	1902-0022	Diode, Breakdown, 2.67V	04713	SZ10939-16
CR2, 3, 7, 8	1910-0030	Diode, Ge, 100 mA, 0.65V	28480	1910-0030
CR4	1910-0022	Diode, Ge, 5 WIV	14433	G401
CR5	1901-0460	Diode, Si, 3 junction stabistor	03508	STB523
L2, 3	9140-0082	Coil, Fxd, RF, 15 uH	28480	9140-0082
Q1, 2, 3	1854-0094	Transistor, Si, NPN	80131	2N3646
Q4, 5	1854-0215	Transistor, Si, NPN	80131	2N3904
Q6, 7	1853-0036	Transistor, Si, PNP	80131	2N3906
Q8, 9	1853-0058	Transistor, Si, PNP	80131	2N3644
Q10, 11, 12	1854-0071	Transistor, Si, NPN	28480	1854-0071
R1	0698-3635	Resistor, Fxd, Met Ox, 680 ohms, 5%, 2W	28480	0698-3635
R3, 21, 25	0698-0084	Resistor, Fxd, Flm, 2.15k, 1%, 1/8W	28480	0698-0084
R4	0698-3153	Resistor, Fxd, Flm, 3.83k, 1%, 1/8W	28480	0698-3153
R5	0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421
R6	0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274
R7, 29	0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132
R8, 27, 31	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442
R9, 45	0698-3155	Resistor, Fxd, Flm, 4.64k, 1%, 1/8W	28480	0698-3155
R10	0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154
R11, 28, 38, 48	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R12	0698-0090	Resistor, Fxd, Flm, 464 ohms, 1%, 1/2W	28480	0698-0090
R13	1810-0008	Resistor, Network (6 fxd flm resistors)	28480	1810-0008
R14, 15, 17, 18	1810-0020	Resistor, Network (7 fxd flm resistors)	28480	1810-0020
R16	0757-0344	Resistor, Fxd, Flm, 51.1 ohms, 2%, 1/8W	28480	0757-0894
R22, 24	0698-0085	Resistor, Fxd, Flm, 2.61k, 1%, 1/8W	28480	0698-0085
R23, 26	0757-0200	Resistor, Fxd, Flm, 5.62k, 1%, 1/8W	28480	0757-0200
R30	0757-1078	Resistor, Fxd, Flm, 1.47k, 1%, 1/2W	28480	0757-1078
R32 (revision 1117)	0757-0461	Resistor, Fxd, Flm, 68.1k, 1%, 1/8W	28480	0757-0461
R32 (revision 1120)	0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154
R33 (revision 1117)	0757-0446	Resistor, Fxd, Flm, 15k, 1%, 1/8W	28480	0757-0446
R33 (revision 1120)	0757-0427	Resistor, Fxd, Flm, 1.5k, 1%, 1/8W	28480	0757-0427
R34	0575-0439	Resistor, Fxd, Flm, 6.81k, 1%, 1/8W	28480	0757-0439
R35	0698-3152	Resistor, Fxd, Flm, 3.48k, 1%, 1/8W	28480	0698-3152
R36	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R37	0698-3151	Resistor, Fxd, Flm, 2.87k, 1%, 1/8W	28480	0698-3151
R43	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R44	0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R46, 47	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
U14, 17, 27	1820-0956	Integrated Circuit, CTL	07263	SL3459
U15	1820-0069	Integrated Circuit, TTL	01295	SN4344
U16, 25, 34, 36, 45, 46, 55, 56, 76, 86, 94, 104	1820-0054	Integrated Circuit, TTL	01295	SN4342
U24, 26, 35, 44	1820-0068	Integrated Circuit, TTL	12040	SN7140N
U41, 42	1820-0099	Integrated Circuit	01295	SN7493N
U54, 66, 84	1820-0071	Integrated Circuit, TTL	01295	SN7440N
U64, 65, 74, 75	1820-0075	Integrated Circuit, TTL	01295	SN4353
U85, 95, 105, 114, 115, 124, 125	1820-0077	Integrated Circuit, TTL	01295	SN4354
U96, 106, 116, 126, 127	1820-0974	Integrated Circuit, CTL	07263	SL4817
W1, 2, 7	8159-0005	Jumper Wire	28480	8159-0005
XY1	1200-0199	Socket, Crystal	28480	1200-0199
Y1	0410-0421	Crystal, Quartz, 225.280 kHz, 0.01%	28480	0410-0421



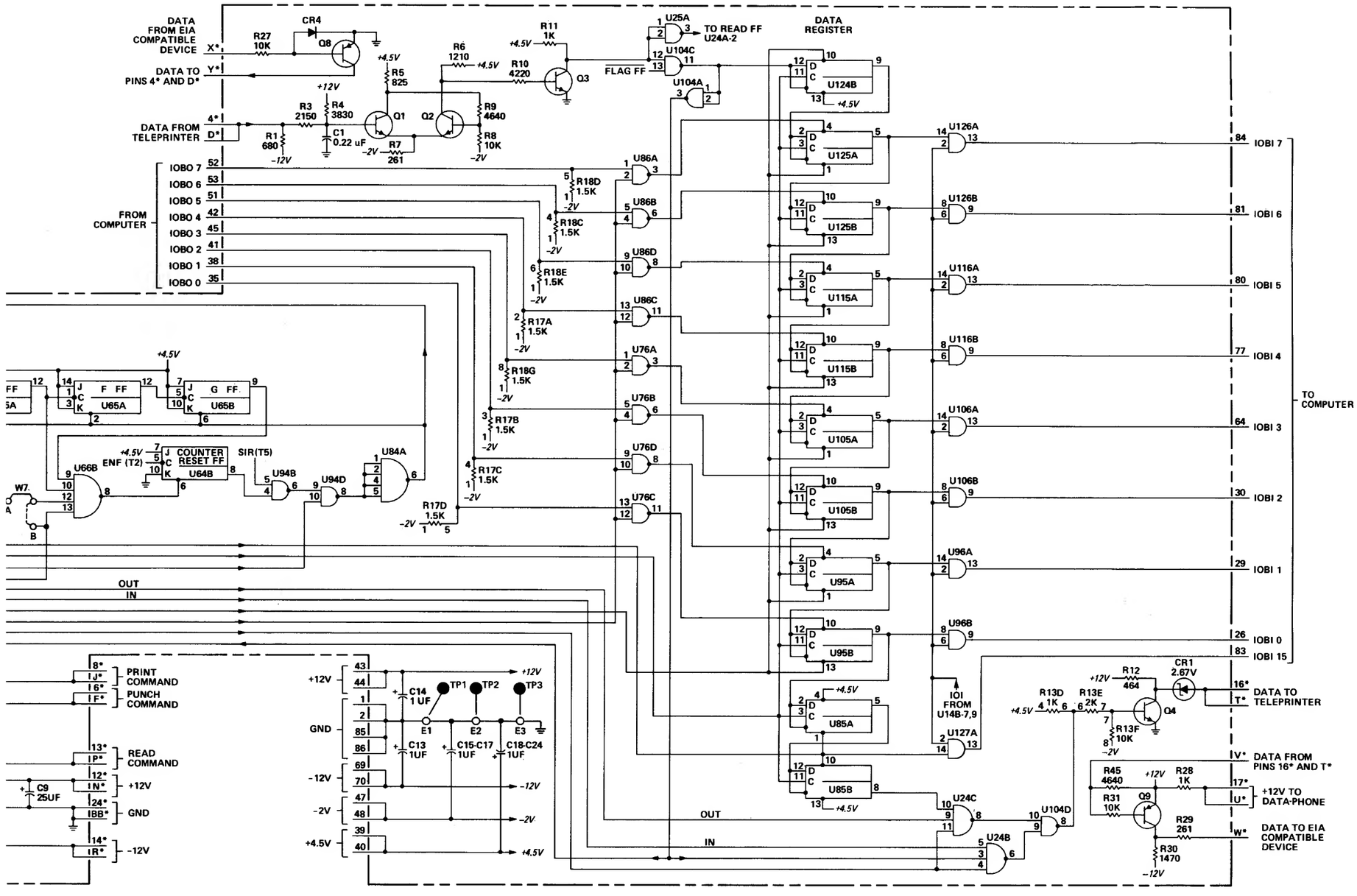
CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOCIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	2.0	0.8	2.4	0.4	Logic 1	29	15
7	2.0	0.8	2.4	0.4	Logic 1	50	50
8	2.0	0.8	2.4	0.4	Logic 1	35	50
17	1.25	0.5	2.25	-0.36	Logic 0	18	18
22	1.5	0.4	2.2	-0.3	Logic 0	24	24
29	2.0	0.8	2.4	0.4	Logic 1	135	135

2154-12

Figure 5-1. Integrated Circuit Pin Connections and Characteristics

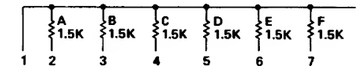
BUFFERED TELEPRINTER INTERFACE CARD (12531-60022, REV. 1117, 1120, AND 1204)

DWG REV. J

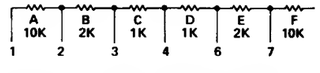


NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN PICOFARADS UNLESS OTHERWISE SPECIFIED.
2. THE ABBREVIATION BPS MEANS BITS-PER-SECOND
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R14, R15, AND R17 THRU R19.



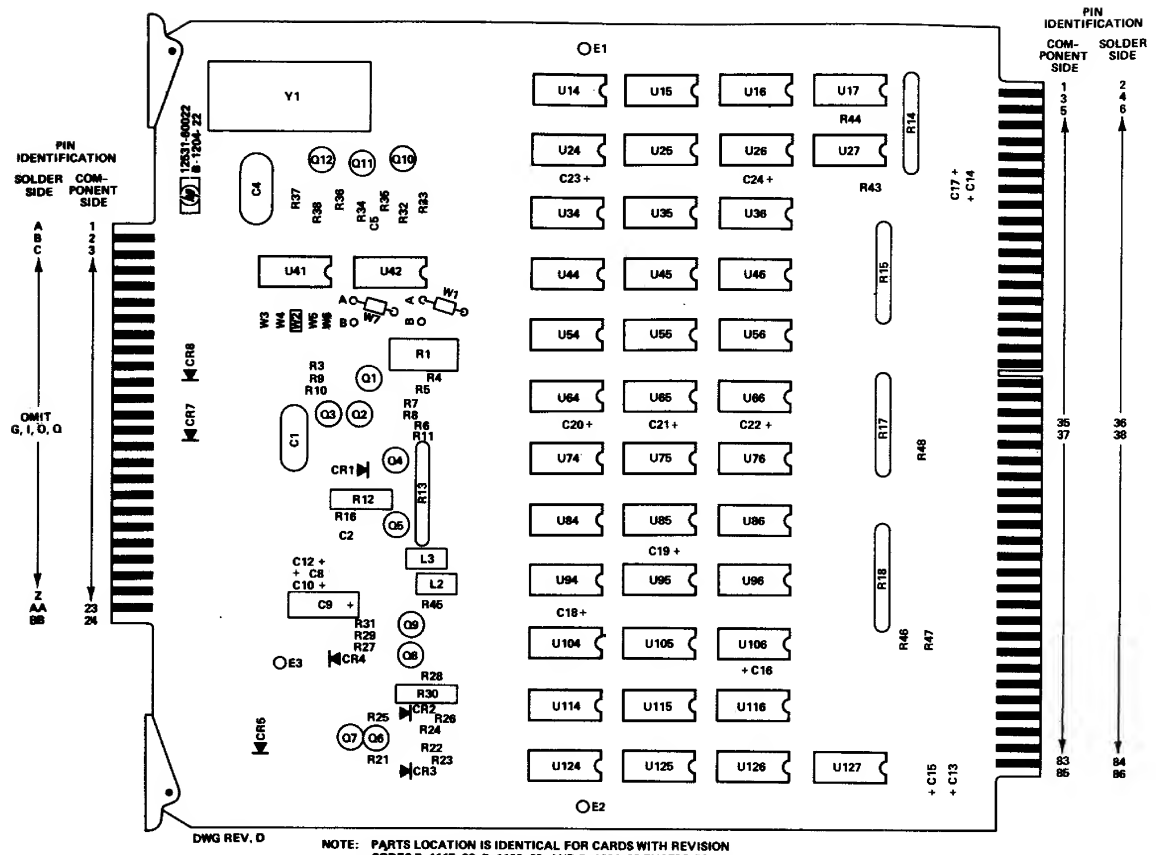
4. SCHEMATIC DIAGRAM FOR RESISTOR NETWORK R1



5. AN ASTERISK (*) DENOTES PINS ON THE 48-PIN CONNECTOR. ALL OTHER PINS ARE ON THE 86-PIN CONNECTOR.
6. ON CARDS WITH REVISION CODE 1117, R32 IS 68.1K AND R33 IS 15K.
7. JUMPER W7 IS INCLUDED ON CARDS WITH REVISION CODE 1204 AND ABOVE.

Figure 5-2. Buffered Teleprinter Interface C Parts Location and Logic Diagra

12531C



NOTE: PARTS LOCATION IS IDENTICAL FOR CARDS WITH REVISION CODES B- 1117- 22, B- 1120- 22, AND B- 1204- 22 EXCEPT FOR JUMPER W7. JUMPER W7 IS ON CARDS WITH REVISION CODE B- 1204- 22 AND ABOVE.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section provides information for ordering replacement parts for the 12531C Buffered Teleprinter Interface Kit.

6-3. Table 6-1 lists parts in numerical order by HP part number and gives the total quantity for each replaceable part in the interface kit. A replaceable parts list (table 5-4) and parts location diagram (figure 5-2) for the interface card are provided in section V of this manual.

6-4. Tables 6-1 and 5-4 list the following information for each part:

a. Reference designation of the part (table 5-4 only). Refer to table 6-3 for an explanation of abbreviations used in the "REFERENCE DESIGNATION" column.

b. Hewlett-Packard part number.

c. Description of the part. Refer to table 6-3 for an explanation of the abbreviations used in the "DESCRIPTION" column.

d. A five digit code that identifies the manufacturer of the part. Refer to table 6-2 for a listing of the manufacturers that correspond to the codes.

e. Manufacturer's part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 6-1 only).

6-5. ORDERING INFORMATION.

6-6. To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Sales and Service Offices are listed at the back of this manual.) Specify the following information for each part ordered:

a. Identification of the instrument, kit, or assembly containing the part (refer to paragraph 1-10).

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation, if applicable.

Table 6-1. Numerical List of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0191	Capacitor, Fxd, Dipped Mica, 56 pf, 5%	28480	0140-0191	1
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	56289	192P10292-PTS	1
0160-0263	Capacitor, Fxd, Cer, 0.22 uF, 20%, 50 VDCW	56289	5C52BS-CML	1
0160-2940	Capacitor, Fxd, Mica, 470 pF, 5%, 300 VDCW	72136	RDM15F471J3C	1
0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X9035A2	17
0180-0338	Capacitor, Fxd, Elect, 25 uF, +75, -10%, 25 VDCW	28480	0180-0338	1
0410-0421	Crystal, Quartz, 225.280 kHz, 0.01%	28480	0410-0421	1
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082	1
0698-0084	Resistor, Fxd, Flm, 2.15k, 1%, 1/8W	28480	0698-0084	3
0698-0085	Resistor, Fxd, Flm, 2.61k, 1%, 1/8W	28480	0698-0085	2
0698-0090	Resistor, Fxd, Flm, 464 ohms, 1%, 1/2W	28480	0698-0090	1
0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132	2
0698-3151	Resistor, Fxd, Flm, 2.87k, 1%, 1/8W	28480	0698-3151	1
0698-3152	Resistor, Fxd, Flm, 3.48k, 1%, 1/8W	28480	0698-3152	1
0698-3153	Resistor, Fxd, Flm, 3.83k, 1%, 1/8W	28480	0698-3153	1
0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154	1
0698-3154**	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154	1
0698-3155	Resistor, Fxd, Flm, 4.64k, 1%, 1/8W	28480	0698-3155	2
0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	1
0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	1
0698-3635	Resistor, Fxd, Met Ox, 680 ohms, 5%, 2W	28480	0698-3635	1
0757-0200	Resistor, Fxd, Flm, 5.62k, 1%, 1/8W	28480	0757-0200	2
0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274	1
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	4
0757-0394	Resistor, Fxd, Flm, 51.1 ohms, 1%, 1/8W	28480	0757-0394	1
0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421	1
0757-0427**	Resistor, Fxd, Flm, 1.5k, 1%, 1/8W	28480	0757-0427	1
0757-0439	Resistor, Fxd, Flm, 6.81k, 1%, 1/8W	28480	0757-0439	1
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442	3
0757-0446*	Resistor, Fxd, Flm, 15.0k, 1%, 1/8W	28480	0757-0446	1
0757-0461*	Resistor, Fxd, Flm, 68.1k, 1%, 1/8W	28480	0757-0461	1
0757-1078	Resistor, Fxd, Flm, 1.47k, 1%, 1/2W	28480	0757-1078	1
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094	2
1200-0199	Socket, Crystal	28480	1200-0199	1
1810-0008	Resistor, Network (6 fxd flm resistors)	28480	1810-0008	1
1810-0020	Resistor, Network (7 fxd flm resistors)	28480	1810-0020	4
1820-0054	Integrated Circuit, TTL	01295	SN4342	12
1820-0068	Integrated Circuit, TTL	12040	SN7410N	4
1820-0069	Integrated Circuit, TTL	01295	SN4344	1
1820-0071	Integrated Circuit, TTL	01295	SN7440N	3
1820-0075	Integrated Circuit, TTL	01295	SN4353	4
1820-0077	Integrated Circuit, TTL	01295	SN4354	7
1820-0099	Integrated Circuit	01295	SN7493N	2
1820-0956	Integrated Circuit, CTL	07263	SL3459	3
1820-0974	Integrated Circuit, CTL	07263	SL4817	5
1853-0036	Transistor, Si, PNP	80131	2N3906	2
1853-0058	Transistor, Si, PNP	80131	2N3644	2
1854-0071	Transistor, Si, NPN	28480	1854-0071	3
1854-0094	Transistor, Si, NPN	80131	2N3646	3
1854-0215	Transistor, Si, NPN	80131	2N3904	2
1901-0460	Diode, Si, 3 junction stabistor	03508	STB523	1
1902-0022	Diode, Breakdown, 2.67V	04713	SZ10939-16	1
1910-0022	Diode, Ge, 5 WIV	14433	G401	1
1910-0030	Diode, Ge, 100 mA, 0.65V	28480	1910-0030	4
8159-0005	Jumper Wire	28480	8159-0005	3
9140-0082	Coil, Fxd, rf, 15 uH	28480	9140-0082	2
12531-60022	Buffered Teleprinter Card	28480	12531-60022	1
12531-90033	Buffered Teleprinter Interface Kit Manual	28480	12531-90033	1

* Revision code 1117 only.
** Revision code 1120 only.

MANUAL PART NO. 12531-90033
MICROFICHE PART NO. 12531-90037

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